A   **Reg. No. :** [ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ]

Question Paper Code: U4303

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2023

Fourth Semester

Electrical and Electronics Engineering

21UEE403-PRINCIPLES OF DIGITAL ELECTRONICS

(Regulations 2021)

Duration: Three hours   Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. How many entries will be in the truth table of a 4-input NAND gate?   CO1- U

   (a) 4   (b) 8   (c) 16   (d) 32

2. Identify the Largest Binary Number that can be expressed with 12 bits?   CO1- U

   (a) $(1111\ 1111\ 1111)_2$ (b) $(4095)_{10}$ (c) $(FFF)_{16}$ (d) All of the above

3. Which pair of Boolean expressions satisfies the idempotency property?   CO1- U

   (a) $A+\overline{A}=1$, $A.\overline{A}=0$ (b) $A+A=A$, $A.A=A$

   (c) $A + 1 = 1$, $A . 1 = A$ (d) $A + 0 = A$, $A . 0 = 0$

4. Find the number of OR gates required to design 8 to 3 encoder circuit   CO1- U

   (a) 3   (b) 5   (c) 8   (d) 16

5. Find the output of SR flip flop when S=1, R=0 is?   CO1- U

   (a) 1   (b) 0   (c)No change   (d) High impedance

6. Which flip-flop will act as Master Slave?   CO1- U

   (a) SR   (b) JK   (c) D   (d) T

7. Internal propagation delay of asynchronous counter is removed by   CO1- U

   (a) Ripple counter   (b) Ring counter

   (c) Modulus counter   (d) Synchronous counter

8. What happens to the parallel output word in an asynchronous binary   CO1- U
   down counter, whenever a clock pulse occurs?

   (a) The output word decreases by 1.   (b) The output word decreases by 2.

   (c) The output word increases by 1.   (d) The output word increases by 2.

9. Find the default value of the reg data type?   CO1- U

   (a) 0   (b) 1   (c) Z   (d) X

10. _____ operator usually comes before the operand   CO1- U

    (a) Unary   (b) Binary   (c) Ternary   (d) None

PART – B (5 x 2= 10Marks)

11. Explain propagation delay.   CO1- U

12. Explaine SOP and POS.   CO1- U

13. Convert JK flip-flop to T flip-flop.   CO1- U

14. Explain the various types of Hazards in sequential circuits.   CO1- U

15. Differentiate blocking and non-blocking assignments.   CO1- U

PART – C (5 x 16= 80Marks)

16. (a) Convert the following   CO1- U   (16)
$$(147.3)_8 \text{ to } (\ )_{16}$$
$$(010010101000)_2 \text{ to } (\ )_{16}$$
$$(38.21)_{10} \text{ to } (\ )_2$$
$$(231.3)_{10} \text{ to } (\ )_8$$
Or

    (b) Explain the types of weighted and non-weighted codes with an   CO1- U   (16)
    example for each .

17. (a) (i) Simplify the following function using K-Map.   CO2- App   (10)
    $F(A,B,C,D)= \sum m(0,1,2,3,4,6,8,9,10,12,14,15)$.
    (ii) Design a half subtractor and implement the same using logic   CO2- App   (6)
    gates.
Or
    (b) (i) Design a Binary to Gray code converter.   CO2- App   (12)
    (ii) Design a half adder and implement the same using logic gates.   CO2- App   (4)

18. (a) Design a synchronous Modulo-10 Up Counter using JK flipflops.   CO2- App   (16)
Or
    (b) Design synchronous sequential circuit that goes through the count   CO2- App   (16)
    sequence 1,3,4,5 repeatedly. Use T flip-flops for your design.

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19. (a) Design an asynchronous sequential circuit with two inputs X1   CO3- App   (16)
and X2 with one output Z. Initially both inputs are equal to '0'.
When X1or X2 becomes '1', the output becomes '1'. When the
second input becomes '1',the output changes to '0'. The output
stays at '0' until the circuit goes back to the initial state.

Or

(b) Implement a 3 X4X2 PLA PLD circuit to implement the logic   CO3- App   (16)
functions $F_1(x,y,z) = \sum m(0,1,3,5)$ $F_2(x,y,z) = \sum m(3,5,7)$

20. (a) Develop Verilog code for full subtractor using gate level and   CO3- App   (16)
data flow modeling.

Or

(b) Develop Verilog code to design 4 bit counter.   CO3- App   (16)

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