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Question Paper Code:R3I05

B.E./B.Tech. DEGREE EXAMINATION, NOV 2025

Third Semester

CSE (Internet of things)

R21UIO305 – COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulations R2021)

Duration: Three hours   Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What is the role of MAR and MDR?   CO1-U

2. Write a program that can evaluate the expression   CO2-App

   A x B + C x D. In a single Accumulator processor. Assume that the processor has Load, Store, Multiply, Add Instructions and that all values fit in the accumulator

3. What is the difference between RISC and CISC?   CO1-U

4. How would you optimize the performance of a basic shift-and-add multiplier in CO2-App
   hardware design?

5. In a 3-stage pipeline (Fetch, Decode, Execute), if instruction I1 is in the CO2-App
   Execute stage and instruction I2 is in the Decode stage, and I2 depends on the
   result of I1, which stage of I2 will be delayed and by how many cycles?

6. Define Pipeline and Characteristics of Pipeline.   CO1-U

7. What are the enhancements used in the memory management?   CO1-U

8. If a cache has a hit rate of 80% and a miss rate of 20%, and the access time for CO2-App
   cache hits is 1 ns and for cache misses is 10 ns, calculate the average memory
   access time.

9. Explain the role of the DMA controller in reducing CPU workload during data CO2-App
   transfers between memory and I/O devices.

10. Define bus.   CO1-U

PART – B (5 x 16= 80 Marks)

11. (a) Describe the operational concepts between the processor and memory.   CO1-U   (16)

Or

(b) Explain in detail the various components of computer system with neat diagram.   CO1-U   (16)

12. (a) Multiply each of the following pairs of signed 2's complement numbers using the Booth Algorithm. And also explain in detail using a flowchart.   CO2-App   (16)
(5) * (-4)

Or

(b) Consider 4-bit dividend and 2 bit divisor, show the steps involved in binary division using restoring methodology and also explain in detail with a flow chart.   CO2-App   (16)
Dividend 1010
Divisor   0011

13. (a) (i) Discuss the basic concepts of pipelining .   CO1- U   (8+8)
(ii) Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome/minimize hazards?

Or

(b) (i) Describe the role of interprocessor communication (IPC) in multiprocessor systems.   CO1- U   (8+8)
(ii) Explain the Cache Coherence.

14. (a) What is virtual memory? Explain the relation between address space and memory space in a virtual memory system along with its memory table for mapping?   CO1- U   (16)

Or

(b) Explain in detail about cache memory?   CO1- U   (16)

15. (a) Configure a DMA controller in an embedded system to efficiently transfer data between a memory location and a peripheral device, addressing specific operational requirements.   CO2-App   (16)

Or

(b) Design a DMA controller circuit that supports both memory-to-memory and I/O-to-memory data transfers.   CO2-App   (16)

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