A **Reg. No. :** | | | | | | | | | | | | |

Question Paper Code: R3303

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2025

Third Semester

Electrical and Electronics Engineering

R21UEE303 – PRINCIPLES OF DIGITAL ELECTRONICS

(Regulations R2021)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. BCD code ranges from CO1- U

   (a) 0 to1 (b) 0 to 9 (c) 0 to 15 (d) 0 to 7

2. MOS transistor is CO1- U

   (a) voltage controlled voltage device (b) current controlled voltage device

   (c) voltage controlled current device (d) current controlled current device

3. Find the number of the gates required to build a half adder are CO1- U

   (a) EX-OR gate and NOR gate (b) EX-OR gate and OR gate

   (c) EX-OR gate and AND gate (d) Four NAND gates

4. Find the number of outputs for 4 input decoder circuit CO1- U

   (a) 2 (b) 16 (c) 4 (d) 5

5. Find the output of D Flip-flop when D=1. CO1- U

   (a) 1 (b) 0 (c) No change (d) X

6. Explain the toggle state in JK Flip-Flop CO1- U

   (a) Set Q = 1 and Q = 0 (b) Set Q = 0 and Q = 1

   (c) Change the output to the opposite state (d) No change in output

7. Internal propagation delay of asynchronous counter is removed by CO1- U

   (a) Ripple counter (b) Ring counter (c) Modulus counter (d) Synchronous counter

8. How much storage capacity does each stage in a shift register represent? CO1- U

(a) One bit (b) two bits (c) four bits (d) eight bits

9. Verilog HDL is a case-sensitive language. All keywords are in CO1-U

(a) lowercase (b) uppercase

(c) either lower or uppercase (d) bold letters

10. The keyword @posedge means CO1- U

(a) Transition from 0 to 1, x or z (b) Transition from x to 1

(c) Transition from z to 1,x (d) All the above

PART – B (5 x 2= 10 Marks)

11. Explain De Morgan's theorem. CO1- U

12. Draw the logic diagram of EX-OR gate using NAND gates. CO1- U

13. Draw the logic diagram of clocked SR flip-flop. Draw the truth table of RS flip flop. CO1- U

14. Implement the following Boolean function using ROM (PROM) CO3- App

$F_1 = \sum m(1,2,3); \quad F_2 = \sum m(0,1,3)$

15. Develop Verilog Code to design half adder using gate level modeling. CO3- App

PART – C (5 x 16= 80 Marks)

16. (a) (i) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8 bit data word that was written in to memory if the 12 bit word read out is as A) 101110010100 B)111111110100 CO1- U (10)

(ii) Convert the following decimal number to hexadecimal, Octal and Binary. (A) $(1259)_{10}$ (B) $(5768)_{10}$ CO1- U (06)

Or

(b) (i) Compare TTL, DTL, RTL and ECL CO1- U (8)

(ii) Draw the CMOS logic circuit for NOR gate. CO1- U (8)

17. (a) (i) Simplify the following function using K-Map. CO2- App (10)

F(A,B,C,D)= ∑ m(0,1,2,3,4,6,8,9,10,12,14,15) .

(ii) Design a half subtractor and implement using logic gates. CO2- App (06)

Or

(b) (i) Simplify the following function using K - Map and implement using gates. F(P,Q,R,S) = ∑ m(0,1,2,4,7,10,11,12) CO2- App (10)

(ii) Design a full adder and implement using logic gates. CO2- App (06)

18. (a) A sequential circuit has two JK Flip-Flops A and B, one input (x) and one output (y). the Flip-Flop input functions are, CO4- Ana (16)

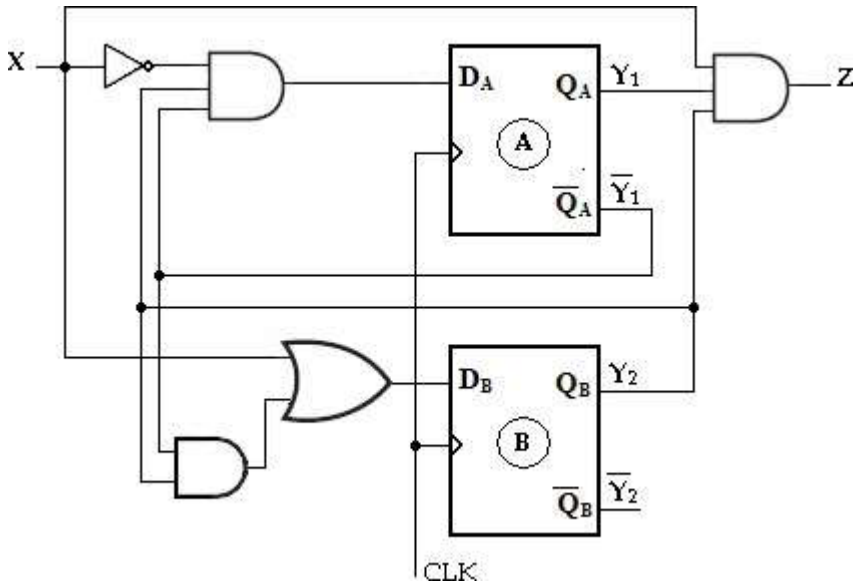
$J_A = B + x \qquad J_B = A' + x'$

$K_A = 1, K_B = 1$

and the circuit output function, $Y = x\,A'$ B. Analyze the synchronous Mealy machine and obtain its state diagram.

Or

(b) Analyze the synchronous Mealy machine and obtain its state diagram. CO4- Ana (16)



19. (a) Design a logic circuit for the following Boolean expression using PROM. CO3- App (16)

$f_1(x, y, z) = \sum m(0,1,2,5,7)$

$f_2(x, y, z) = \sum m(1,2,4,6)$

Or

(b) Develop a PLA circuit to implement the logic function A'BC+AB'C+AC' and A'B'C'+BC CO3- App (16)

20. (a) Develop Verilog code to design 8 to 1 multiplexer using dataflow and behavioral modeling. CO3- App (16)

Or

(b) Write Verilog code to design 3 to 8 decoder using gate level and behavioral modeling. CO3- App (16)

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