C **Reg. No. :** | | | | | | | | | | | | |

Question Paper Code: R3402

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2025

Third Semester

Electronics and Communication Engineering

R21UEC302-DIGITAL ELECTRONICS AND DESIGN

(Regulations R2021)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5Marks)

1. Which of the following gate is called universal gate? CO1-U

   (a) AND (b OR (c) XOR (d) NAND

2. Number of Half Adders and Full Adders required to construct a 64-bit binary adder would be _____ CO2- App

   (a) 1 Half adder and 63 Full adder (b) 64 full adders

   (c) 64 half adders (d) 1 full adder and 63 half adder

3. The characteristic equation of J-K flip-flop is _____ CO1- U

   (a) Q(n+1)=JQ(n)+K'Q(n) (b) Q(n+1)=J'Q(n)+KQ'(n)

   (c) Q(n+1)=JQ'(n)+KQ(n) (d) Q(n+1)=JQ'(n)+K'Q(n)

4. What is/are the crucial function/s of memory elements used in the sequential circuits? CO1- U

   (a) Storage of binary information (b) Specify the state of sequential

   (c) Both (a) & (b) (d) None of the above

5. The full form of PLD is _____ CO1 - U

   (a) Programmable Large Device (b) Programmable Long Device

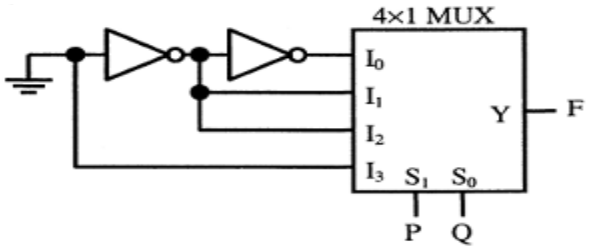
   (c) Programmable Logic Device (d) Programmable Lengthy Device

PART – B (5 x 3= 15 Marks)

6. Convert octal to binary conversions. a) $(376)_8$ b) $(466)_8$ CO2 -App

7. The logic function implemented by the circuit below is CO2 -App

   (ground implies a logic "0")



8. Compare sequential and combinational circuit. CO1 U

9. A traffic signal cycles from GREEN to YELLOW, YELLOW to RED and RED to GREEN. In each cycle, GREEN is turned on for 70 seconds, YELLOW is turned on for 5 seconds and the RED is turned on for 75 seconds. This traffic light has to be implemented using a finite state machine (FSM). The only input to this FSM is a clock of 5 second period. The minimum number of flip-flops required to implement this FSM is _____. CO2-App

10. Differentiate static and dynamic RAM. CO1-U

PART – C (5 x 16= 80 Marks)

11. (a) Find a minimal SoP and PoS for the expression y= $\sum m$ (3,4,5,7,9,13,14,15) using Karnaugh map method. CO2 -App (16)

Or

(b) Implement the following function F=ab+bc+ac using basic gates and universal Gates CO2 -App (16)

12. (a) Design a combinational circuit which has three inputs and produces two outputs using logic gates. CO2 -App (16)

Or

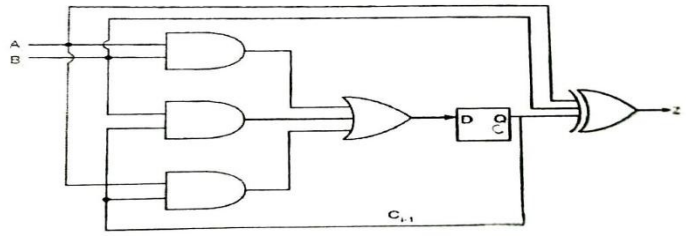
(b) Implement the Boolean function using 8:1 multiplexer $f(A,B,C,D) = \sum m(1,3,4,11,12,13,14,15)$. CO2 -App (16)

13. (a) Design a counter with the following sequence using T flipflop 0000, 0010, 0100, 0110, 1000, 1010, 1100, 1110, 0000 CO2 -App (16)

Or

(b) Design a synchronous Mod 6 UP counter using JK flipflops CO2 -App (16)

14. (a) Inspect the operation of a synchronous sequential circuit designed as a serial adder to add two 4-bit binary numbers. The circuit uses D and T flip-flops for storage and control. Examine the role of each flip-flop type in the design and explain how the circuit processes the inputs over clock cycles. CO3– Ana (16)



Or

(b) Design a serial binary adder using D flip flops and T flip flop for the numbers 1011 and 0110 and also justify your answer. CO3– Ana (16)

15. (a) Design a Binary-to-Gray converter similar to basic ROM Structure. CO2 -App (16)

Or

(b) Design a BCD (Binary-Coded Decimal) to Excess-3 code converter using read only memory architecture CO2 -App (16)