Reg. No. : | | | | | | | | | | | | |

Question Paper Code:R9478

B.E./B.Tech. DEGREE EXAMINATION, NOV 2025

Open Elective

R21UEC978 CMOS FABRICATION USING SEMULATOR 3D

(Regulations R2021)

(Common to All Engineering Branches)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1.	Differentiate NMOS and PMOS transistors.	CO1- U	
2.	Explain the purpose of wafer cleaning in VLSI fabrication.	CO1- U	
3.	Explain the concept of bird's beak in fabrication.	CO1- U	
4.	Discuss gate-first in MOSFET fabrication	CO1- U	
5.	Distinguish Dry etch and wet etch.	CO1- U	
6.	Classify the types of photoresist.	CO1- U	
7.	Distinguish Physical Vapour Deposition (PVD) and Chemical Vapour Deposition (CVD).	CO1- U	
8.	Discuss the advantage of Atomic Layer Deposition (ALD)	CO1- U	
9.	Illustrate the FINFET inverter.	CO1- U	
10.	Why are High-k materials used in advanced MOSFET fabrication?	CO1- U	

PART – B (5 x 16= 80 Marks)

11.	(a)	Illustrate the complete CMOS fabrication process with neat diagrams.	CO1- U	(16)
		Or		
	(b)	Show the CMOS logic for 2 input NAND gate and explain its function for each logical input.	CO1- U	(16)
12.	(a)	Make use the concept of STI to create an oxidation layer and explain it.	CO2- App	(16)
		Or		

	(b)	Apply the concepts of epitaxial growth in forming epi-layer in CMOS fabrication and explain its process and importance	CO2- App	(16)
13.	(a)	A silicon wafer needs selective oxide removal—apply an appropriate wet etchant for this task.	CO2- App	(16)
		Or		
	(b)	Apply dry etching techniques to minimize undercutting compared to wet etching.	CO2- App	(16)
14.	(a)	A wafer undergoes diffusion at 1000 °C for 2 hours with a diffusion coefficient of 3×10^{-13} cm^2/s. Apply Fick's law to calculate the junction depth.	CO3- App	(16)
		Or		
	(b)	Apply the concept of doping to design a silicon wafer with a resistivity of 5Ω·cm. Calculate the required doping concentration and explain the steps.	CO3- App	(16)
15.	(a)	A chip shows increased RC delay due to interconnect scaling. Apply metallization and dielectric solutions to minimize this delay.	CO3- App	(16)
		Or		
	(b)	Design FinFET device architecture to overcome short-channel effects. Compare FinFET with conventional MOSFET using diagrams.	CO3- App	(16)