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Question Paper Code: R4809

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2025

Professional Elective

Electronics and Communication Engineering

R21ECV509 - CMOS ADVANCED MICRO FABRICATION USING SEMULATOR 3D

(Regulations R2021)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1.	Explain NMOS and PMOS transistors.	CO1-U
2.	Interpret the design rules in CMOS layout.	CO1-U
3.	Differentiate between LOCOS and STI.	CO1-U
4.	Explain about gate dielectric. Give an examples.	CO1-U
5.	Explain about reactive ion etching (RIE).	CO1-U
6.	Summarize about a mask aligner to copy a circuit pattern onto a silicon wafer during photolithography.	CO1-U
7.	Distinguish between PVD and CVD.	CO1-U
8.	Illustrate about ALD. Where is it used?	CO1-U
9.	Illustrate the various fabrication steps (like doping, deposition, and lithography) to ensure proper functioning and yield of a CMOS device	CO1-U
10.	Summarize any one reliability challenge in advanced CMOS.	CO1-U

PART – B (5 x 16= 80 Marks)

11.	(a)	Explain the CMOS fabrication process with neat diagrams.	CO1 U	(16)
		Or		
	(b)	Explain the purpose of design rules in IC layout. How do these rules help in avoiding manufacturing defects during fabrication?	CO1 U	(16)
12.	(a)	Discuss the advantages of using high-k/metal gate over traditional gate materials.	CO1-U	(16)
		Or		
	(b)	Explain the challenges in integrating Hi-K materials in nanoscale CMOS.	CO1-U	(16)

13.	(a)	Explain the lithography process in IC fabrication.	CO1-U	(16)
		Or		
	(b)	Explain how multiple patterning overcomes the limitations of traditional lithography.	CO1-U	(16)
14.	(a)	What is annealing? Describe its role in activation.	CO1-U	(16)
		Or		
	(b)	With neat diagrams, describe the process of Physical Vapor Deposition (PVD). List different PVD techniques and their applications.	CO1-U	(16)
15.	(a)	Apply the concept of electromigration and explain how it influences interconnect design and material choice in sub-10nm technology nodes.	CO3-App	(16)
		Or		
	(b)	Elucidate how dual damascene processing is applied in multilayer interconnects. What makes it preferable over traditional subtractive etching methods?	CO3-App	(16)