A		Reg. No. :										
<b>Question Paper Code: R2804</b>												
B.E./B.Tech. DEGREE EXAMINATION, NOV 2024												
Second Semester												
Information technology												
R21UIT204 - DIGITAL PRINCIPLES & SYSTEM DESIGN												
(Regulations R2021)												
Dur	ation: Three hours							Max	imuı	n: 10	0 M	arks
Answer ALL Questions												
		PART A - (	10 x 1	= 10 M	arks)							
1.	Find 2's complement of	of(11000100) <sub>2</sub>									CO2	2-App
	a) (00111100) <sub>2</sub>	b) (111111) <sub>2</sub>	С	e) (1100	010) <sub>2</sub>	2			d) (1	11110	)101	)2
2.	What is the output of t	that $A + \overline{AB} =$									CO2	2-App
	(a) A+B	(b) B+A	(	c) A+A					(d) /	A+B		
3.	The result obtained on	binary multiplicat	tion of	1010*1	100 is	s					CO2	2-App
	(a) 1111000	(b) 1111001	(	c) 1111	000				(d) 1	11110	)01	
4.	The Simplified express	sion of full subtrac	tor Bo	orrow is							C	01 <b>-</b> U
	(a) $B_{out} = \overline{AB}_{in} + \overline{AB} + B_{in}$	B <sub>in</sub>		(b) B <sub>out</sub>	=BA	in+BB	+B.	A <sub>in</sub>				
	(c) $B_{out} = AB_{in} + BA + AA$	Lin		$(d) AB_{d}$	in+BE	B <sub>in+</sub> BE	<b>B</b> <sub>in</sub>					
5.	If the number of m requiresselected	-	lines	is equ	ial to	52 <sup>m</sup> 1	then	it			C	01 <b>-</b> U
	(a) n	(b) m	(	c) 2					(d) 2	2n		
6.	For re programmability	y, PLDs use									C	01 <b>-</b> U
	(a) PROM	(b) EPROM	(	a) PRO	Μ				(d) I	De M	ultip	lexer
7.	The functional differen	nce between SR fli	ip-flop	and JK	flip-f	lop is	that	t			C	01 <b>-</b> U
	(a) JK flip-flop is faste	o (ł	(b) JK flip-flop has a feedback path									
	(c) JK flip-flop accepts	(0	(d) JK flip-flop does not require external clock									

8.	A counter circuit is usually constructed of	CO1-U										
	(a) A number of latches connected in cascade form											
	(b) A number of NAND gates connected in cascade form											
	(c) A number of flip-flops connected in cascade											
	(d) A number of NOR gates connected in cascade form											
9.	A condition occurs when an asynchronous sequential circuit changes two or more binary states variable is	C	CO1-U									
	(a) deadlock condition (b) Running condition (c) Race condition	(d) None										
10.	The race in which stable state depends on order is called	C	CO1-U									
	(a) critical race (b) identical race (c) non critical race	(d) defined race										
	PART - B (5 x 2 = 10 Marks)											
11.	Identify the 2's complement of the following: (i) 1111111 (i) 101010	CO2-App										
12.	Derive the K-map and draw the logic diagram of full-adder	CO2-App										
13.	Draw the truth table and circuit diagram of 4 to 2 encoder.	CO2-App										
14.	Construct the Excitation table for J-K Flip flop	CO2-App										
15.	Outline on Hazards and its effect on circuit	CO2-App										
	PART – C (5 x 16= 80Marks)											
16.	(a) Minimize the expression using QuineMccluskey method: $Y = \overline{AB}\overline{C}\overline{D} + \overline{AB}\overline{C}D + AB\overline{C}\overline{D} + AB\overline{C}D + A\overline{B}\overline{C}D + \overline{AB}\overline{C}\overline{D}$	CO2-App (	(16)									
	Or											
	(b) Simplify the following Boolean Expression:	CO2-App (	(16)									
	i) $Y = AB + A(B + C) + B(B + C)$ (4)											
	ii) $Y = \overline{AB}(\overline{A} + B)(\overline{B} + B)$ (4)											
	iii) $\overline{Y = \overline{A}\overline{C} + \overline{B}\overline{C} + B\overline{C} + ABC} $ (4)											
	iv) $\overline{Y = A + \overline{A}B + \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C}D}$ (4)											
17.	<ul> <li>(a) Derive the truth table for full adder and simplify the K-map for its outputs. Draw its block schematic and logic diagram of sum of product (SOP) implementation of full adder.</li> <li>Or</li> </ul>	CO2-App (	(16)									
	(b) Design a logic circuit to convert BCD to grav code	$CO_2$ App (	(16)									

(b) Design a logic circuit to convert BCD to gray code. CO2-App (16)

18. (a) Realize  $F(w,x,y,z) = \sum (1,4,6,7,8,9,10,11)$  using 4 to 1 MUX. CO2-App (16)Or (b) Design a switching circuit that converts a 4 bit binary code into a 4 CO2-App (16)bit Gray code using ROM array Construct a S-R Flip-Flop with 2-bit input values 00,01,10 & 11 CO2-App 19. (a) (16)and reclaim its states necessary logic diagram (b) Design divide by 6 counter using T-flip-flops. Write state table and CO2-App (16)reduce the expression using K-map Design an asynchronous sequential circuit with two inputs x1 and CO2-App 20. (a) (16)x2 and one output Z. Initially both inputs are equal to zero. When x1 or x2 becomes 1 the output Z becomes 1. When the second input also becomes 1 the output changes to 0. The output stays at 0 until the circuit goes back to the initial state.

(b) Give hazard– free realization for the following Boolean function CO2-App (16)  $F(A,B,C,D) = \sum (0,2,4,5,8,10,14)$  $f(A,B,C,D) = \pi (3,4,7,8,9,12,15)$ 

Or

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