	Reg. N	0. :											
						40.04							
Question Paper Code: 94805													
	B.E./B.Tech. DEC	GREE	EXAI	MIN	ATI	ON, I	NOV	V 202	24				
		Fourt	h Sen	neste	er								
	In	formati	ion te	chno	logy	7							
	19UIT405- COMPUTER	ORGA	NIZA	ATIC)N A	ND	AR	СНІЛ	ТЕСТ	UR	E		
		(Regul	ations	s 201	9)								
Dura	ation: Three hours							Max	imur	n: 1(00 Ma	rks	
	А	nswer	All Q	uest	ions								
	PAR	ТА-(10x 2	= 20) Ma	rks)							
1.	What is Instruction Register (IR) and Program Counter (PC) used for?						С	CO1- U					
2.	What are the two techniques used to increase the clock rate R?						С	CO1- U					
3.	What is full adder?						С	CO1- U					
4.	What are the ways to truncate the guard bits?						С	CO1- U					
5.	List the state elements needed to store and access an instruction.						CO1- U						
6.	Define register file.						CO1- U						
7.	Draw the basic structure of Basic Multiprocessor	Structu	ure of	a Sy	ymm	etric	Sha	red 1	Mem	ory	С	:01-	U
8.	What is Instruction Level Paralleli	sm?									CO1- U		
9.	Consider a direct-mapped cache w Byte address 1200 will map to bloc	vith 64 ck num	block 1ber	s and	d a b	lock of th	size e ca	of 1 che.	6 by	tes.	CO2- App		
10.	For a disk rotating at 10,000 rp rotational delays?	om, wh	at ar	e th	e ma	axim	um	and	aver	age	CC)2- A	pp
	PA	RT – E	B (5 x	16=	= 801	Mark	s)						
11.	(a) Explain the functional unit of detail.	f a com	nputer	wit	h the	bloc	ck d	iagra	m in	C	D1-U		(16
		Or											
	(b) What is an addressing mode?	Explai	n var	ous	addr	essin	g m	odes	in	C	D1-U		(1e)

detail with example and neat diagram for each.

12.	(a)	Perform the integer division for the number 8/3 using restoring division	CO2-App	(16)				
Or								
	(b)	Multiply given signed 2's complement numbers using bit pair recoding A=110011 (Multiplicand) B=101100 (Multiplier).	CO2-App	(16)				
13.	(a)	Write the basic MIPS implementation of instruction set. Or	CO2-App	(16)				
	(b)	Examine the approaches would you use to handle exceptions in MIPS	CO2-App	(16)				
14.	(a)	 Consider a non-pipelined machine with 6 execution stages of lengths 50 ns, 50 ns, 60 ns, 60 ns, 50 ns, and 50 ns. 1. Find the instruction latency on this machine. 2. How much time does it take to execute 100 instructions? Or 	CO2-App	(16)				
	(b)	How fast execution can we expect from a parallel computer for a concrete application?	CO2-App	(16)				
15.	(a)	Describe the data transfer method using DMA. Or	CO1- U	(16)				
	(b)	Write the basic operations of cache in detail with diagram	CO1- U	(16)				