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Reg. No. : | | | | | | | | | | | | |

**Question Paper Code: R2I04**

B.E./B.Tech. DEGREE EXAMINATION, MAY 2024

Second Semester

CSE (Internet of things)

R21UIO204- DIGITAL SYSTEM AND DESIGN

(Regulations R2021)

Duration: Three hours | Maximum: 100 Marks

Answer All Questions

PART A - (10 x 1 = 10 Marks)

1. The logical expression for $Y=A+\overline{A}B$ CO2-App

   (a) A+B (b) 1 (c) (1 + AB) (d) A

2. The minterm is also known as _____ CO1-U

   (a) SOP (b) POS

   (c) Hybrid (d)Both SOP and POS

3. The simplified expression of full adder carry is _____ CO1-U

   (a) c = xy+xz+yz (b) c = xy+xz (c) c = xy+xz+yz (d) c = xy+yz

4. Convert Gray code 1110 to binary_____ CO2-App

   (a) 1011 (b) 1111 (c) 1011 (d) 1111

5. The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called _____ CO1-U

   (a) Combinational circuits (b) Sequential circuits

   (c) Latches (d) Flip-flops

6. In magnitude comparator ,If two numbers are not equal then the binary value will be CO2-App

   (a) 0 (b) 1 (c) 2 (d) 3

7. The table that is not a part of the asynchronous analysis procedure is _____ CO1-U

   (a) transition table (b) state table

   (c) low table (d) Excitation table

8. Time delay device is the memory element of CO1-U

(a) Unclocked flip-flops (b) clocked flip-flops

(c) synchronous circuits (d) asynchronous circuits

9. In a computer, registers are present _____ CO1-U

(a) Within control unit (b) Within RAM

(c) Within ROM (d) Within CPU

10. SPLDs, CPLDs, and FPGAs are all which type of device? CO1-U

(a) PAL (b) PLD (c) EPROM (d) SRAM

PART – B (5 x 3= 15 Marks)

11. Identify the 2's complement of the following: CO2-App

(i) 1111111

(ii) 101010

12. Draw the truth table for full-subtractor. CO2-App

13. Draw the logic diagram for T Flip Flop. CO1-U

14. Define hazard. CO1-U

15. Give any two application of PLA. CO1-U

PART – C (5 x 15= 75 Marks)

16. (a) (i) Prove the following Boolean expressions. (8Marks) CO2-App (15)

(a) $A + AB = A$

(b) $A + \overline{A}B = A + B$

(c) $(A + B)(A + C) = A + BC$

(ii) Implement F= $\overline{A}B + A\overline{B})(C + \overline{D)}$ using NOR gates.

(8Marks)

Or

(b) Simplify the following function using tabulation method. CO2-App (15)
Implement it using simple logic gates

F(A,B,C,D)=∑ m(1,4,6,7,8,9,10,11,15)

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| 17. | (a) | Design a 4 bit binary to gray code converter. | CO2-App | (15) |
| | | Or | | |
| | (b) | Design a logic circuit to convert BCD to gray code | CO2-App | (15) |
| 18. | (a) | Design a look ahead carry adder with necessary diagrams. | CO2-App | (15) |
| | | Or | | |
| | (b) | Design and explain about 1-Bit and 2-Bit Comparator. | CO2-App | (15) |
| 19. | (a) | Develop Verilog program for full adder using structural model | CO2-App | (15) |
| | | Or | | |
| | (b) | An asynchronous sequential circuit is described by the following excitation and output function:<br>$Y = X_1X_2 + (X_1 + X_2)Y,$<br>$Z = Y$<br>(i) Draw the logic diagram of the circuit<br>(ii) Derive the transition table and output map<br>(iii) Describe the behaviour of the circuit | CO2-App | (15) |
| 20. | (a) | (i) Draw a dynamic RAM cell and explain its operation with neat diagram. (8Marks)<br>(ii) Explain about Static and dynamic RAM (8Marks) | CO1-U | (15) |
| | | Or | | |
| | (b) | Explain in detail about FPGA and also the types of FPGA. | CO1-U | (15) |