A **Reg. No. :** | | | | | | | | | | | | |

Question Paper Code: R3303

B.E./B.Tech. DEGREE EXAMINATION, NOV 2024

Third Semester

Electrical and Electronics Engineering

R21UEE303 - PRINCIPLES OF DIGITAL ELECTRONICS

(Regulations R2021)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. How many entries will be in the truth table of a 4-input NAND gate? CO1- U

   (a) 4 (b)8 (c)16 (d) 32

2. Identify the Largest Binary Number that can be expressed with 12 bits? CO1- U

   (a) $(1111\ 1111\ 1111)_2$ (b) $(4095)_{10}$ (c) $(FFF)_{16}$ (d) All of the above

3. Which pair of Boolean expressions satisfies the idempotency property? CO1- U

   (a) $A+\overline{A}=1$, $A.\overline{A}=0$ (b) A+A=A, A . A=A

   (c) A + 1 = 1, A . 1 = A (d) A + 0 = A, A . 0 = 0

4. Find the number of outputs for 4 input decoder circuit CO1- U

   (a) 2 (b) 16 (c) 4 (d) 5

5. Explain the toggle state in JK Flip-Flop CO1- U

   (a) Set Q = 1 and Q = 0 (b) Set Q = 0 and Q = 1

   (c) Change the output to the opposite state (d) No change in output

6. An 8 bit register is used to store CO1- U

   (a) 8 bit data (b) 16 bit data (c) 8 byte data (d) 2 byte data

7. Internal propagation delay of asynchronous counter is removed by CO1- U

   (a) Ripple counter (b) Ring counter (c) Modulus counter (d) Synchronous counter

8. What happens to the parallel output word in an asynchronous binary down counter whenever a clock pulse occurs? CO1- U

(a) The output word decreases by 1. (b) The output word decreases by 2.

(c) The output word increases by 1. (d) The output word increases by 2.

9. Verilog HDL is a case-sensitive language. All keywords are in CO1- U

(a) lowercase (b)uppercase (c) either lower or uppercase (d) bold letters

10. Find the default value of the reg data type? CO1- U

(a) 0 (b) 1 (c) Z (d) X

PART – B (5 x 2= 10 Marks)

11. Distinguish RTL and DTL CO1- U

12. Convert the given expression in canonical SOP form Y = AB + A'C + BC' CO2- App

13. Draw SR Flipflop using gates. CO1- U

14. Why is the pulse mode operation of asynchronous sequential circuits not very popular? CO1- U

15. Develop Verilog Code to design half adder using gate level modeling. CO2- App

PART – C (5 x 16= 80 Marks)

16. (a) Convert the following CO1- U (16)

$(147.3)_8$ to $(\ )_{16}$

$(010010101000)_2$ to $(\ )_{16}$

$(38.21)_{10}$ to $(\ )_2$

$(231.3)_{10}$to $(\ )_8$

Or

(b) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8 bit data word that was written in to memory if the 12 bit word read out is as A) 101110010100 B)111111110100 CO1- U (16)

17. (a) i) Design a Binary to Gray code converter. CO2- App (12)

ii) Design a half adder and implement using logic gates. CO2- App (4)

Or

(b) i) Design a 8:1 Multiplexer using logic gates. CO2- App (8)

ii) Design a 4 to 2 encoder circuit using logic gates. CO2- App (8)

18.	(a)	Design a sequence detector to detect the sequence 1001 using JK flip-flops.	CO2- App	(16)
		Or		
	(b)	Design a synchronous Modulo-10 Up Counter using JK flipflops.	CO2- App	(16)
19.	(a)	Implement the following function using PAL F1 (A, B, C) = Σ(1, 2, 4, 6); F2 (A, B, C) = Σ(0, 1, 6, 7); F3 (A, B, C) = Σ(1, 2, 3, 5, 7).	CO3- App	(16)
		Or		
	(b)	Develop a PLA circuit to implement the logic function A'BC+AB'C+AC' and A'B'C'+BC	CO3- App	(16)
20.	(a)	Develop Verilog code to design 8 to 1 multiplexer using dataflow and behavioral modeling.	CO3- App	(16)
		Or		
	(b)	Develop Verilog Code to design full adder using gate level and behavioural modeling.	CO3- App	(16)