A **Reg. No. :** | | | | | | | | | | | | |

Question Paper Code: U4303

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2024

Fourth Semester

Electrical and Electronics Engineering

21UEE403-PRINCIPLES OF DIGITAL ELECTRONICS

(Regulations 2021)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Identify the even parity code from the following CO1- U

   (a) 11001 (b) 1110 (c) 0111 (d)0110

2. Calculate the ($)_2$ equivalent of$(125)_8$ CO1- U

   (a) 1010101 (b) 1001001 (c) 11001100 (d) 111000

3. Which pair of Boolean expressions satisfies the idempotency property? CO1- U

   (a) $A+\overline{A}=1$, $A.\overline{A}=0$ (b) A+A=A, A . A=A

   (c) A + 1 = 1, A . 1 = A (d) A + 0 = A, A . 0 = 0

4. Find the number of OR gates required to design 8 to 3 encoder circuit CO1- U

   (a) 3 (b)5 (c) 8 (d) 16

5. Find the output of SR flip flop when S=1, R=0 is? CO1- U

   (a) 1 (b)0 (c)No change (d) High impedance

6. Which flip-flop will act as Master Slave? CO1- U

   (a) SR (b) JK (c) D (d) T

7. Internal propagation delay of asynchronous counter is removed by CO1- U

   (a) Ripple counter (b) Ring counter

   (c) Modulus counter (d) Synchronous counter

8. What happens to the parallel output word in an asynchronous binary down counter, whenever a clock pulse occurs? CO1- U

(a) The output word decreases by 1. (b) The output word decreases by 2.

(c) The output word increases by 1. (d) The output word increases by 2.

9. The Verilog HDL code starts with the keyword CO1- U

(a) always (b)module (c)endmodule (d) items

10. Find the default value of the reg data type? CO1- U

(a) 0 (b) 1 (c) Z (d) X

PART – B (5 x 2= 10Marks)

11. Explain propagation delay. CO1- U

12. Explain SOP and POS. CO1- U

13. Explain the drawback of SR Flip-flop. CO1- U

14. Draw PLA Structure. CO1- U

15. Differentiate blocking and non-blocking assignments. CO1- U

PART – C (5 x 16= 80Marks)

16. (a) Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction (a) X-Y and (b) Y-X using 2's Complement and also using 1's Complement. CO1- U (16)

Or

(b) i) Explain Error Detection and Error correction codes with an example. CO1- U (12)

ii) Explain alphanumeric codes. (4)

17. (a) (i) Simplify the following function using K-Map. CO2- App (10)

$F(A,B,C,D)= \sum m(0,1,2,3,4,6,8,9,10,12,14,15)$.

(ii) Design a half subtractor and implement the same using logic gates. CO2- App (6)

Or

(b) (i) Design a Binary to Gray code converter. CO2- App (12)

(ii) Design a half adder and implement the same using logic gates. CO2- App (4)

18. (a) Design a synchronous Modulo-7 Up Counter using JK flipflops CO2- App (16)

Or

(b) Design and implement the various types of shift registers. CO2- App (16)

19.	(a)	Develop a PLA circuit to implement the logic function A'BC+AB'C+AC' and A'B'C'+BC	CO3- App	(16)
		Or		
	(b)	Implement the following function using PAL F1 (A, B, C) = Σ(1, 2, 4, 6); F2 (A, B, C) = Σ(0, 1, 6, 7); F3 (A, B, C) = Σ(1, 2, 3, 5, 7).	CO3- App	(16)
20.	(a)	Develop Verilog code to design Demultiplexer and Decoder by using	CO3- App	(16)
		Or		
	(b)	Develop Verilog Code to design 8 to 3 Encoder using gate level and data flow modeling.	CO3- App	(16)