A **Reg. No. :** | | | | | | | | | | |

Question Paper Code: 94303

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2024

Fourth Semester

Electrical and Electronics Engineering

19UEE403 – Principles of Digital Electronics

(Regulations 2019)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Choose the another name of base CO1- U

   (a) Foundation (b) radix (c) subscript (d) none

2. Identify the even parity code from the following CO1- U

   (a) 11001 (b) 1110 (c) 0111 (d)0110

3. What will be the number of selection lines in a 16 to 1 Multiplexer? CO1-U

   (a) Type- 0 (b) Type -1 (c) Type -2 (d) Type - 3

4. Find the number of the gates required to build a half adder are CO1- U

   (a) EX-OR gate and NOR gate (b) EX-OR gate and NOR gate

   (c) EX-OR gate and AND gate (d) Four NAND gates

5. What is the output of SR flip flop when S=1, R=0 is? CO1- U

   (a) 1 (b) 0 (c) No change (d) High impedance

6. What is output of D Flipflop when D=1? CO1- U

   (a) 1 (b)0 (c) No Change (d) X

7. How many natural states will there be in a 4-bit ripple counter? CO1- U

   (a) 4 (b) 8 (c) 16 (d) 32

8. How much storage capacity does each stage in a shift register represent? CO1- U

(a) One bit (b) two bits (c) four bits (d) eight bits

9. Metal links are made up of CO1- U

(a) Polycrystalline (b) Magnesium sulphide (c) Nichrome (d) Silicon dioxide

10. Which of the following loops are supported by verilog? CO1- U

(a) if-else loop (b) for loop (c) while loop (d) All the above

PART – B (5 x 2= 10 Marks)

11. Classify the types of Binary Codes based on positional weighting CO1- U

12. Define SOP and POS. CO1- U

13. Define a sequential logic circuit. Give an example. CO1- U

14. Define Races . CO1- U

15. Define CPLD and FPGA. CO1- U

PART – C (5 x 16= 80Marks)

16. (a) (i) Encode the binary word 1011 in to seven bit Hamming code. CO1- U (10)

(ii) Evaluate Excess 3 code and gray code for $(F)_H$ and $(AB)_H$ CO1- U (6)

Or

(b) Explain the types of weighted and non-weighted codes with an example for each type. CO1- U (16)

17. (a) (i) Simplify the following function using K - Map and implement using gates. $F(A,B,C,D) = \sum m(0,1,2,3,4,5,7,10,11,12,15)$ CO2- App (8)

(ii) Design a full subtractor and implement using logic gates. CO2- App (8)

Or

(b) (i) Implement the given function using 8 X 1 MUX $F(A,B,C,D) = \sum m(0, 1,2, 6,7,8,9,10,11,12,15)$ CO2- App (8)

(ii) Design 3 to 8 decoder using logic gates. CO2- App (8)

18. (a) Design a synchronous Modulo-10 Up Counter using JK flip flops. CO2- App (16)

Or

(b) Design synchronous sequential circuit that goes through the count sequence 1,3,4,5 repeatedly. Use T flip-flops for your design. CO2- App (16)

19. (a) Design an asynchronous sequential circuit with two inputs X1 and X2 with one output Z. Initially both inputs are equal to '0'. When X1or X2 becomes '1', the output becomes '1'. When the second input becomes '1',the output changes to '0'. The output stays at '0' until the circuit goes back to the initial state. CO4- App (16)

Or

(b) Develop the state diagram and primitive flow table for a logic system that has two inputs X and Y and a single output Z. which is to behave in the following manner. Initially, both the inputs and Outputs are equal to 0.Whenever X=1 and Y=0, the Z becomes 1 and whenever X=0 and Y=1 The Z becomes 0.When inputs are zero; X=Y= 0 or inputs X=Y=1, the Z doesn't change it remains in the previous state. State input values are not to have any effect in changing the Z output. CO4- App (16)

20. (a) Implement a 3 X4X2 PLA PLD circuit to implement the logic functions CO2- App (16)

$F_1(x,y,z) = \sum m(0,1,3,5)$ $F_2(x,y,z) = \sum m(3,5,7)$

Or

(b) Develop Verilog code for full adder using gate level and data flow modeling. CO2- App (16)

94303