Reg. No. : | | | | | | | | | | | | |

Question Paper Code: U6402

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2024

Sixth Semester

Electronics and Communication Engineering

21UEC602 - VLSI DESIGN

(Regulations 2021)

Duration: Three hours | Maximum: 100 Marks

PART A - (5 x 1 = 5Marks)

1. The possible signal values in Verilog HDL are _____ CO1- U

   (a) 2 (b) 5 (c) 4 (d) 11

2. The distance between the source and drain is called CO1- U

   (a) Channel (b) Gate (c) Drain (d) Source

3. The resistance and capacitance product of the MOS transistor is called CO1- U

   (a) intrinsic delay (b) Extrinsic delay (c) both a & b (d) none

4. In positive logic convention, the true state is represented as CO1- U

   (a) 1 (b) 0 (c) -1 (d) -0

5. Gate capacitance per unit area is scaled by CO1- U

   (a) α (b)1 (c) $1/\beta$ (d) β

PART – B (5 x 3= 15Marks)

6. Design a D flip-flop circuit using behavioral level description. CO2 - App
7. What are the different operating modes of MOS transistor? CO1- U
8. Why does interconnect increase the circuit delay? CO1 – U
9. Design the AND gate using pseudo NMOS logic. CO3 - App
10. State the Application of Adiabatic logic. CO1 – U

PART – C (5 x 16= 80Marks)

11.	(a)	Explain the VLSI design flow of Verilog HDL.	CO1 – U	(16)
		Or		
	(b)	Explain design methodology and hierarchy model with suitable example.	CO1 – U	(16)
12.	(a)	Design the OUT=(AB+CD)' using CMOS layout design rules.	CO1 – U	(16)
		Or		
	(b)	Derive the expression for minimum possible delay of an N-stage path.	CO1 – U	(16)
13.	(a)	Discuss the different reliability problems related to the design of reliable chips.	CO1 – U	(16)
		Or		
	(b)	Discuss the principle of constant field scaling and also write its effect on device characteristics.	CO1 – U	(16)
14.	(a)	Design latches and flip-flops using CMOS circuits.	CO2 – App	(16)
		Or		
	(b)	Explain the concept of modified booth multiplier with suitable examples.	CO2 – App	(16)
15.	(a)	Analyze the Different voltage scaling method using to design low power CMOS Circuits.	CO1 – U	(16)
		Or		
	(b)	Analyze different voltage scaling methods for low power design influence of voltage scaling on power and delay.	CO1 – U	(16)