Reg. No. : | | | | | | | | | | | | |

Question Paper Code :R3B02

B.E./B.Tech. DEGREE EXAMINATION, NOV 2024

Third Semester

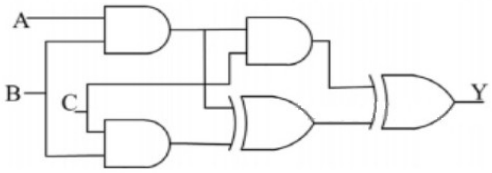
Biomedical Engineering

R21UBM302-DIGITAL LOGIC CIRCUITS

(Regulations R2021)

Duration: Three hours | Maximum: 100 Marks

PART A - (10 x 2 = 20 Marks)

1.	Implement Boolean expression for EX - OR gate using NAND gates only.	CO2-App
2.	State De-Morgan's theorem.	CO1-U
3.	The output of the combinational circuit given below is 	CO2-App
4.	Why carry look ahead adder is faster than ripple carry adder and full adder?	CO1-U
5.	How many flip-flops are required to build a binary counter that counts from 0 to 7?	CO1-U
6.	Distinguish between synchronous counter and asynchronous counter.	CO1-U
7.	Define Hazards and How it can be avoided?	CO1-U
8.	Classify Asynchronous sequential circuits.	CO1-U
9.	Why RAMs are called as Volatile?	CO1-U
10.	How programmable logic devices are classified?	CO1-U

PART – B (5 x 16= 80 Marks)

11.	(a)	Plot the following logical Expression on a 4-variable K – map F=ABCD+AB'C'D'+AB'C+AB & realize the SOP using only NAND gates and POS using only NOR gates.	CO2-App	(16)
		OR		
	(b)	Find a minimal sum–of–products for the Boolean expression $f(w,x,y,z) = \sum m(1,2,3,7,8,9,10,11,14,15)$ using various methods and justify your answer.	CO2-App	(16)

12.	(a)	(i) Discuss about the design of 4-bit BCD adder with neat diagram and mention how many adders are used in the BCD circuit	CO2-App	(8)
		(ii) Analyze the principle and design of Parallel binary adder with diagrams.	CO2-App	(8)
		OR		
	(b)	(i)Implement the following functions using Multiplexers. $F(A,B,C,D)= \sum m(0,1,3,4,8,9,15)$	CO2-App	(8)
		(ii) Draw the logic diagram of binary to octal decoder and explain the working in detail.	CO2-App	(8)
13.	(a)	(i) Design for a 4-bit ring counter using J-K flip flops and D flip flop and justify your answer.	CO3-App	(8)
		(ii) Realize D flip-flop using SR flip-flop.	CO1-U	(8)
		OR		
	(b)	(i) Design MOD 6 Unit distance counter using JK flip-flop.	CO3-App	(8)
		(ii) Describe the operation of universal shift register with neat block diagram.	CO1-U	(8)
14.	(a)	Design an asynchronous sequential circuit with two input A and B and one output C. Initially both inputs are equal to zero. When A or B becomes 1 the output C becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuits goes back to the initial state.	CO4-App	(16)
		OR		
	(b)	(i) Design a sequence detector that produces an output 1 whenever the sequence 101101 is detected.	CO4-App	(10)
		(ii) Design a circuit that has no static hazards and implement the Boolean function $F(A,B,C,D) = \Sigma (0,2,6,7,8,10,12)$ using AND-OR logic.	CO4-App	(6)
15.	(a)	Implementation the following Boolean function using PAL. $W(A,B,C,D)=\sum m(0,2,6,7,8,9,12,13)$ $X(A,B,C,D)=\sum m(0,2,6,7,8,9,12,13,14)$ $Y(A,B,C,D)=\sum m(2,3,8,9,10,12,13)$ $Z(A,B,C,D)=\sum m(1,3,4,6,9,12,14)$	CO5-App	(16)
		OR		
	(b)	Design PLA, PAL realizations of a full-adder with inputs A, B, C and outputs Sum and Carry.	CO5-App	(16)