Reg. No. : | | | | | | | | | | |

Question Paper Code: 94805

B.E./B.Tech. DEGREE EXAMINATION, NOV 2022

Fourth Semester

Information technology

19UIT405- COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulations 2019)

Duration: Three hours Maximum: 100 Marks

Answer All Questions

PART A - (10x 2 = 20 Marks)

1.	What is Instruction Register (IR) and Program Counter (PC) used for?	CO1- U
2.	What are the two techniques used to increase the clock rate R?	CO1- U
3.	What is full adder?	CO1- U
4.	What are the ways to truncate the guard bits?	CO1- U
5.	Define MIPS.	CO1- U
6.	Give the format of MIPS R-type instruction.	CO1- U
7.	Draw the basic structure of Basic Structure of a Symmetric Shared Memory Multiprocessor	CO1- U
8.	What is Instruction Level Parallelism?	CO1- U
9.	Define memory cycle time.	CO2- App
10.	Specify the three types of the DMA transfer techniques?	CO2- App

PART – B (5 x 16= 80Marks)

11.	(a)	Compare 0,1,2 and 3 address machines by writing a program to compute: X=(A+BxC)/(D-ExF-GxH)	CO2-App	(16)

Or

	(b)	An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (i) direct; (ii) immediate; (iii) relative (iv) register indirect; (v) index with R1 register as the index register.	CO2-App	(16)
12.	(a)	Perform the integer division for the number 8/3 using restoring division	CO2-App	(16)
		Or		
	(b)	Multiply given signed 2's complement numbers using bit pair recoding A=110011 (Multiplicand) B=101100 (Multiplier).	CO2-App	(16)
13.	(a)	Write the basic MIPS implementation of instruction set.	CO2-App	(16)
		Or		
	(b)	Examine the approaches would you use to handle exceptions in MIPS	CO2-App	(16)
14.	(a)	Consider a non-pipelined machine with 6 execution stages of lengths 50 ns, 50 ns, 60 ns, 60 ns, 50 ns, and 50 ns. 1. Find the instruction latency on this machine. 2. How much time does it take to execute 100 instructions?	CO2-App	(16)
		Or		
	(b)	How fast execution can we expect from a parallel computer for a concrete application?	CO3- Ana	(16)
15.	(a)	Write the virtual memory and its importance wit neat diagram.	CO1- U	(16)
		Or		
	(b)	Express mapping schemes used in cache memory. (i) Direct (ii) Associate (iii) Set associate	CO1- U	(16)