

Question Paper Code: 59310

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2021

Elective

Electrical and Electronics Engineering

15UEE910– VLSI Design and Architecture

(Regulation 2015)

Duration: Three hours

Maximum: 100 Marks

PART A - (10 x 2 = 20 Marks)

Answer Any ten of the Following Questions

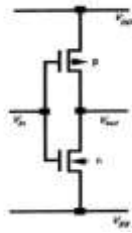
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|-----|--|----------|
| 1. | Explain the impact of mobility degradation and velocity saturation. | CO1 - U |
| 2. | Compare NMOS& PMOS Transistor. | CO1 - U |
| 3. | Write the Current Equation of NMOS transistor which operates in Saturation in region | CO1– U |
| 4. | Define design margin. | CO2 –R |
| 5. | Recommend some methods to reduce dynamic power dissipation. | CO2 – An |
| 6. | List various sources of leakage currents. | CO2 – R |
| 7. | List out the techniques used for low power logic design. | CO3 –R |
| 8. | Compare latch and Filp-flop. | CO3 – U |
| 9. | Define Clock skew and clock jitter. | CO3 – R |
| 10. | Compare CLA with RCA. | CO4 –U |
| 11. | Why do we prefer Booth’s Algorithm ? | CO4- U |
| 12. | List out the components of datapath. | CO4 – R |
| 13. | What are the types of conditional statements in Verilog? | CO5 – R |
| 14. | List out the bitwise operators in Verilog. | CO5 – R |
| 15. | Compare module and instance. | CO5 - U |

PART – B (5 x 16= 80Marks)

16. (a) Summarize the non-ideal I-V characteristics of MOS Transistor with necessary equations. CO1 - U

Or

(b) Illustrate the working of the given circuit in various operating regions based on V_{in} the input voltage levels with necessary equations and diagrams.



17. (a) Sketch a static CMOS gate computing $Y = \text{complement}[(A + B + C) \cdot D]$. CO2 - App
 Or
 (b) Design 2:1 Multiplexer using Transmission gate. CO2 - App
18. (a) Explain the operation of True Single Phase Clocked Register. CO3 - U
 Or
 (b) Explain the concept of timing issues and pipeline. CO3 - U
19. (a) Design a 4 bit full adder using Carry look ahead adder. CO4 - App
 Or
 (b) Design 16 bit carry bypass and carry select adder and discuss their features CO4 - App
20. (a) Develop verilog code to design 3 - bit Encoder using data flow modeling. CO5 - C
 Or
 (b) Develop Verilog code to design 4 - bit Encoder using behavioural modeling. CO5 - C