Reg. No. : | | | | | | | | | | |

Question Paper Code: 43402

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2021

Third Semester

Electronics and Communication Engineering

14UEC302 – DIGITAL ELECTRONICS AND DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The binary equivalent of decimal 41 is

   (a) 101001 (b) 101010 (c) 010111 (d) 101101

2. The simplified logic of the Boolean function $x'y'z + x'yz + xy'$ is

   (a) $x'yz+xyz$ (b) $x'z + xy'$ (c) $x'z'+ x'y'$ (d) $xz+xy$

3. The difference output of half-subtractor is

   (a) $x'y'+ xy$ (b) $xy+xy'$ (c) $xy+xy'$ (d) $x'y+xy'$

4. The circuit that generates the parity bit in the transmitter is

   (a) Parity checker (b) Parity generator

   (c) Both (a) and (b) (d) None of these

5. Which latch is called a transparent latch

   (a) SR latch (b) JK latch (c) D latch (d) T latch

6. How many flip-flops are needed for a 4-bit counter?

   (a) 2 (b) 3 (c) 4 (d) 6

7. The voltage needed for a TTL IC power supply is

(a) 5V dc (b) 10 V dc (c) 2 V dc (d) 20 V dc

8. Which of the following memories in non-volatile memory?

(a) ROM (b) PROM
(c) Ferrite core memory (d) None of these

9. A circuit which do not operate in synchronous with clock signal is

(a) Synchronous sequential circuits (b) Asynchronous sequential circuits
(c) FPGA (d) combinational circuits

10. In this mode the inputs and outputs are represented by levels

(a) Fundamental mode (b) Pulse mode
(c) Both (a) and (b) (d) None of these

PART - B (5 x 2 = 10 Marks)

11. Obtain the canonical sum of product form of the function: $Y=AB + ACD$.

12. Draw the 4-bit binary divider.

13. Write the excitation table of RS flip-flop.

14. Draw the circuit diagram of a TTL-NAND gate with totem pole output.

15. List the design procedure of Asynchronous sequential circuits.

PART - C (5 x 16 = 80 Marks)

16. (a) Realize the following function as Multilevel NAND –NAND gate and Multilevel NOR –NOR gate

$F = \overline{A}\,B + B\,(C + D) + E\overline{F}\,(\overline{B} + \overline{D})$ (16)

Or

(b) (i) Simplify the Boolean function using K-map

$F\,(w, x, y, z) = \Sigma\,(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$. (8)

(ii) Implement the following function with NAND gate only

$F\,(x, y, z) = \Sigma\,(0, 6)$. (8)

17. (a) (i) With logic diagram Truth table and explain about 3-to-8 decoder. (6)

(ii) Define multiplexer and implement the Boolean function with a suitable multiplexer.

$F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$. (10)

Or

(b) With Truth table, design BCD-to-excess-3 code converter and obtain its logic diagram. (16)

18. (a) (i) With neat diagram explain in detail about how the race around condition is avoided in master-slave JK flip-flop. (8)

(ii) Design 4-bit asynchronous up-down binary counter using T flip-flop. (8)

Or

(b) (i) Realize D flip-flop using SR flip-flop. (8)

(ii) With neat illustration explain in detail about 4-bit parallel-in-serial out shift register. (8)

19. (a) With block diagram explain about PLA and realize the following functions in PLA:

$$F1 = \overline{A}\ B\ \overline{C} + A\ \overline{B}\ C + \overline{A}\ B\ C$$

$$F2 = A\ B + A\ C + \overline{A}BC$$

(16)

Or

(b) (i) Differentiate registered PAL and configurable PAL (8)

(ii) Design a 4-bit binary–to gray code converter using PROM. (8)

20. (a) (i) Develop VHDL code for 3 to 8 decoder. (8)

(ii) Explain the method to eliminate static hazard in an asynchronous circuit with an example. (8)

Or

(b) Design serial binary adder using D-flip-flop. (16)

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