Reg. No. : | | | | | | | | | | |

Question Paper Code: 33402

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2021

Third Semester

Electronics and Communication Engineering

01UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Convert the decimal number 34.435 to binary.
2. State De Morgan's theorems. Simplify the expression Y(A,B,C,D) = [A(B+C')'D]' using it.
3. Draw the logic diagram of a half subtractor with inputs X, Y and outputs D, M using gates.
4. What is data selector?
5. Mention the problems faced by ripple counter.
6. Mention the problems faced by ripple counter.
7. What is the difference between PAL and PLA?
8. List the different types of memory.
9. What is the difference between synchronous and asynchronous sequential circuits?
10. Distinguish between static and dynamic hazards.

PART - B (5 x 16 = 80 Marks)

11. (a) (i) What are maxterms and minterms? Express Y(A,B,C) = AB + A'C as a sum of minterms. (10)

(ii) Using K map find the minimized expression for the following function F(w,x,y,z) = Σ(0,2,4,5,6,7,8,10,13,15). (6)

Or

(b) Simplify the following function using tabulation method.
$f(A, B, C, D) = \sum m(2, 3, 7, 9, 11, 13) + \sum d(1, 10, 15)$ (16)

12. (a) (i) Implement the full subtractor using a 1: 8 demultiplexer. (6)

(ii) Implement the following Boolean function using 16:1 multiplexer $f(A, B, C, D, E) = \sum m(2, 4, 5, 7, 10, 14, 15, 16, 17, 25, 26, 30, 31)$ (10)

Or

(b) Implement the following Boolean function using 16:1 multiplexer $f(A, B, C, D, E) = \sum m(2, 4, 5, 7, 10, 14, 15, 16, 17, 25, 26, 30, 31)$. (16)

13. (a) (i) Narrate the operating principle of master slave JK flip flop. (6)

(ii) Design a MOD-6 synchronous counter using J-K Flip-Flops. (10)

Or

(b) Design 3 bit binary counter using T flip flop. Give the state table, state diagram and logic diagram. (16)

14. (a) With neat diagram explain the RAM organization. (16)

Or

(b) Narrate the operation of 2 input CMOS NAND and NOR gates. (16)

15. (a) Narrate the different types of Hazards. Discuss in detail how the hazards can be eliminated. (16)

Or

(b) Illustrate with an example the hierarchical modeling concepts used in Verilog HDL. (16)