Reg. No. : | | | | | | | | | | |

Question Paper Code: 33506

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2021

Third Semester

Electronics and Instrumentation Engineering

01UEI306 – DIGITAL ELECTRONICS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What are the different classifications of binary codes?
2. Reduce A'B'C' + A'BC' + A'BC
3. What is priority encoder?
4. What do you mean by comparator?
5. Define sequential circuit.
6. Differentiate between edge triggering and level triggering.
7. Differentiate fundamental mode and pulse mode asynchronous sequential circuits.
8. Define hazards.
9. Compare PROM and EPROM.
10. Draw the basic configuration of PLA.

PART - B (5 x 16 = 80 Marks)

11. (a) Simplify the given Boolean function into

    (i) Sum of products form (8)

    (ii) Product of sum form and implement it using basic gates. $F(A, B, C, D) = \Sigma (0, 1, 2, 5, 8, 9, 10)$. (8)

Or

(b) Given Y (A, B, C, D) = ∏M (0, 1, 3, 5, 6, 7, 10, 14, 15), draw the K-map and obtain the simplified expression and realize using basic gates (16)

12. (a) (i) Realise (8)

(a) $Y = A + BC\overline{D}$ Using NAND gate.

(b) $Y = (A + C)(A + \overline{D})(A + B + \overline{C})$ Using NOR gates.

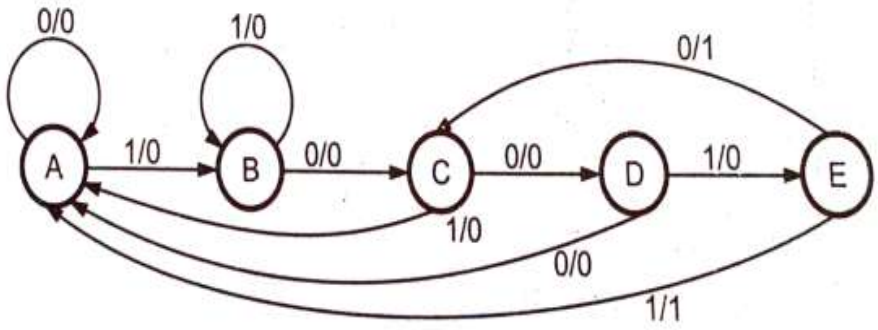
(ii) Implement the Boolean function using 8:1 MUX.
$F(P, Q, R, S) = \sum m(0,1,3,4,8,9,15)$ (8)

Or

(b) Design a BCD to Excess-3 converter using truth table and k-map simplification. (16)

13. (a) (i) Explain how a J-K flip-flop can be converted into a D flip-flop. (8)

(ii) Design a sequential circuit using D flip-flop for the given state diagram. (8)



Or

(b) Design a 3-bit synchronous counter which counts in the sequence 000, 001, 011, 010,100, 110, (repeat) 000 using D flip flop. (16)

14. (a) Design an asynchronous sequential circuit with two inputs x_1 and x_2 and one output *Z*. The output *Z*=1 if x_1 changes from 0 to 1 , *Z*=0 if x_2 changes from 0 to 1, and *Z*=0 otherwise. Realize the circuit using JK flip-flop. (16)

Or

(b) Design a asynchronous circuits that will produce output only the first pulse received and ignore if any other pulses. (16)

15. (a) Explain in detail about the architecture of PLA with a specific example. (16)

Or

(b) Implement the following function using PLA. $F_1 (x, y, z) = \sum m (1, 2, 4, 6)$; $F_2 (x, y, z) = \sum m (0, 1, 6, 7)$; $F_3 (x, y, z) = \sum m (2, 6)$. (16)