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Question Paper Code: 37504

B.E. / B.Tech. DEGREE EXAMINATION, DEC 2021

Seventh Semester

Electronics and Instrumentation Engineering

01UEI704 - VLSI SYSTEM DESIGN

(Regulation 2013)

Duration: Three hours

Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What is body effect?
2. What are the advantages of Twin-tub process?
3. Define short channel devices.
4. Indicate the different symbols used for various regions in stick diagram.
5. What are the advantages of AOI implementation of two level logic functions?
6. What are the advantages of AOI implementation of two level logic functions?
7. What factors determine the overall size of a PLA?
8. Mention some of PLDs.
9. List out the operators in VHDL.
10. Write the behavioral VHD L code for a full adder.

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Show the various components of nMOS transistor model. (6)
(ii) Elaborate the process and steps involved in CMOS Fabrication of VLSI system technology. (10)

Or

- (b) Explain the operation of MOS transistor in depletion mode and enhancement mode. (16)

12. (a) Explain the DC characteristics and switching characteristics of a CMOS inverter. (16)

Or

- (b) Derive the expression for 4:1 and 8:1 pull up and pull down ratios of nMOS inverter. (16)

13. (a) (i) What is Barrel shifter and discuss its SHIFT-1 and SHIEFT-2 operation. (8)
(ii) Discuss about dynamic CMOS. (8)

Or

- (b) (i) Construct an AOI CMOS equivalent for the sum of products expression
 $Y = ABC + ADE + EFG$. (16)

14. (a) (i) Explain the NMOS NAND-NAND PLA realization with a neat stick diagram. (8)
(ii) Discuss about the design of complex PLA. (8)

Or

- (b) (i) Explain the architecture of any one type of FPGA. (8)
(ii) Write short notes on floor planning and placement. (8)

15. (a) (i) Explain a simple test bench for any one Flip-Flop with necessary VHDL code. (8)
(ii) Write the structural VHDL code for 5-bit synchronous counter. (8)

Or

- (b) Write the VHDL code for Finite State Machine using behavioral and structural modeling. (16)