Reg. No. : | | | | | | | | | | |

Question Paper Code: 43306

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2022

Third Semester

Electrical and Electronics Engineering

14UEE306 – DIGITAL LOGIC CIRCUITS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Convert hexadecimal value 16 to decimal.

   (a) 22 (b) 16 (c) 10 (d) 20

2. The propagation delay of TTL is

   (a) 10ns (b) 120ns (c) 200ns (d) None of these

3. The output of an exclusive-NOR gate is 1. Which input combination is correct?

   (a) A=1, B=0 (b)A=0, B=1 (c) A=0, B=0 (d) none of these

4. AND-OR realization is equivalent to

   (a) SOP (b) POS (c) K-map (d) None of these

5. The terminal count of a typical modulus-10 binary counter is

   (a) 0000 (b) 1010 (c) 1001 (d) 1111

6. How many flip-flops are required to make a MOD-32 binary counter?

   (a) 3 (b) 4 (c) 5 (d) 6

7. Which type of PLD should be used to program basic logic functions?

(a) PLA (b) PAL (c) CPLD (d) SLD

8. Which of the statement is true about static-1 hazard?

(a) output goes momentarily goes to 0 when it should remain at 1
(b) output goes momentarily goes to 1 when it should remain at 0
(c) output changes 3 or more times
(d) none of these

9. A combinational circuit that selects one from many inputs

(a) encoder (b) decoder
(c) multiplexer (d) demultiplexer

10. One application of a digital multiplexer is to facilitate

(a) data generation (b) serial-to-parallel conversion
(c) parity checking (d) data selector

PART - B (5 x 2 = 10 Marks)

11. Determine $(377)_{10}$ in Octal and Hexa-Decimal equivalent.

12. Design a half subtractor.

13. Differentiate between Mealy and Moore models.

14. What is a hazard?

15. List the data objects supported by VHDL.

PART - C (5 x 16 = 80 Marks)

16. (a) Given that a frame with bit sequence 1101011011 is transmitted, it has been received as 1101011010. Determine the method of detecting the error using any one error detecting code. (16)

Or

(b) (i) Convert 1010111011101100_2 into octal, decimal and hexadecimal equivalent. (8)

(ii) List the advantages of digital ICs. (8)

17. (a) (i) Simplify the following function using Karnaugh map.

$f(w,x,y,z)=\sum(0,1,3,9,10,12,14)+\sum d(2,5,6,11)$ (8)

(ii) Implement the following function using only NAND gates.

$f(x,y,z)=\sum m(0,2,4,6)$ (8)

Or

(b) Minimize the following Boolean function using K map

$F = \Sigma m\ (0, 2, 5, 7, 8, 10, 13, 15, 16, 21, 23, 24, 26, 29) + \Sigma d(1, 9, 18, 30, 31)$ (16)

18. (a) Design BCD asynchronous counter with state table and state diagrams. (16)

Or

(b) (i) Design a serial adder using Mealy state model. (8)

(ii) List and explain the steps used for analyzing a synchronous sequential circuit. (8)

19. (a) Describe the steps involved in design of asynchronous sequential circuit in detail with an example. (16)

Or

(b) (i) An asynchronous sequential circuit is described by the following excitation and output function.

$Y=x_1\ x_2'+(x_1 + x_2')y$

$Z=y$

(1) Draw the logical diagram of the circuit

(2) Derive the transition table and output map.

(3) Obtain flow table. (8)

(ii) Implement the following function using PLA $F_1 = \sum m\ (4,5,7)$ and

$F_2 = \sum m\ (3,5,7)$. (8)

20. (a) Explain in detail the RTL design procedure. (16)

Or

(b) Write a VHDL description of a D flip flop. (16)