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**Question Paper Code: 44304** 

## B.E. / B.Tech. DEGREE EXAMINATION, MAY 2022

Fourth Semester

Electrical and Electronics Engineering

14UEE404 - ANALOG INTEGRATED CIRCUITS

(Common to Instrumentation and Control Engineering)

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

**Answer ALL Questions** 

PART A -  $(10 \times 1 = 10 \text{ Marks})$ 

- 1. In Monolithic IC
  - (a) Performance depends on the substrate
  - (b) Performance does not depend on the substrate
  - (c) Performance depends on interconnects
  - (d) Performance depends on packaging

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<i>Z</i> .	now many	reads does in	e TO-5 metal can	package of an o	perational am	pimer na	ive

- (a) 8, 10, or 12
- (b) 6, 8, or 10
- (c) 8 or 14
- (d) 8 or 16

- 3. Specified value of CMRR for 741 opamp is
  - (a) 30 dB
- (b) 40 dB
- (c) 90 dB
- (d) 120 dB
- 4. What is the scale multiplier (factor) of a basic integrator?
  - (a) R/C
- (b) C/R

- (c) -RC
- (d) 1/RC

5.	In applications where measurement of a circuit recommended is	physical quantity is involved, the Op-amp							
	(a) Basic non-inverting amplifier	(b) A comparator							
	(c) An active filter	(d) An instrumentation amplifier							
6.	5. In a sample and hold circuit the following statement is false								
	<ul><li>(a) Sample time is much smaller than hold time</li><li>(b) Aperture time is the delay between the time that the pulse is applied to the switch and the actual time the switch closes</li><li>(c) Acquisition time is the time it takes for the capacitor to charge from one voltage to another voltage</li><li>(d) The voltage across the hold capacitor changes by 50% during hold time</li></ul>								
7.	Which of the following techniques are used	for the analog multipliers?							
	(a) Logarithmic multipliers	(b) Variable trans-conductance multipliers							
	(c) Both (a) and (b)	(d) None of these							
8.	How many $V_{cc}$ connections does the 565 PLL use?								
	(a) 0 (b) 1	(c) 2 (d) 3							
9.	. Regulators in which the transistor act in the active region are called								
	(a) linear regulator	<ul><li>(b) switching regulator</li><li>(d) adjustable regulator</li></ul>							
	(c) non linear regulator								
10.	10. Voltage regulator LM7805 has an output voltage of								
	(a) 5 volts (b) -5 volts	(c) 0.5 volts (d) -0.5 volts							
	PART - B (5 x $2 = 10 \text{ Marks}$ )								
11.	1. Why inductors are difficult to fabricate in ICs?								
12.	What is virtual ground?								
13.	3. What is a precision diode?								
14.	4. Enumerate the features of 555 Timer Integrated Circuits.								

15. Mention the limitations of linear IC voltage regulators. What is the order of the voltage drop across the current limiting resistor in an IC regulator when the limiting action occurs.

PART - C (5 x 
$$16 = 80 \text{ Marks}$$
)

16. (a) Mention the dimensions of a typical Integrated Circuits and different types of packaging of IC's. List the steps involved in the manufacturing process of an Integrated Circuits. Discuss the following processes in the monolithic IC technology with necessary diagram wherever necessary.

Or

- b) Briefly explain the various processes involved in the fabrication of monolithic bipolar transistor. (16)
- 17. (a) (i) An IC 741 op-amp whose slew rate is 0.5 V/μs is used as an Inverting Amplifier with a gain of 50. The voltage gain against frequency curve of IC 741 is flat upto 20 kHz. Evaluate what maximum peak to peak signal can be applied without distorting the output.
  - (ii) For a practical integrator, the component values are  $R_1 = 120 \text{ k}\Omega$ ,  $R_F = 1.20 \text{ M}\Omega$  and the capacitor  $C_F = 10 \text{ nF}$ . Draw the circuit diagram. Determine the safe frequency above which true integration will take place and DC gain. Find the peak of the output voltage for a sine wave input with 5 V peak and 10 kHz frequency. Sketch the rough nature of the frequency response.

Or

- (b) (i) The Common Mode Rejection Ratio (CMRR) of an Op-amp is  $10^4$ . Two sets of signals are applied to it. First set is  $V_1$ = + 20  $\mu$ V,  $V_2$  = 20  $\mu$ V and second set  $V_1$ = 540  $\mu$ V,  $V_2$  = 500  $\mu$ V. Calculate the percent difference in output voltage for the two sets of signals.
  - (ii) Design an op-amp differentiator that will differentiate an input signal with  $f_{max} = 100 \text{ Hz}$ . Draw the output waveform for a sine wave of 1 V peak at 100 Hz applied to the differentiator. Also repeat the same for a square wave input. (10)

18.	(a)	(i)	What is an Instrumentation Amplifier? Draw a system whose gain is contriby an adjustable resistance. Name the circuit that is used to detect the peak of the non-sinusoidal waveforms.	
		(ii)	Draw the circuit of a voltage to current converter if the load is floating grounded. Is there any limitation on the size of the load when ground Discuss.	
			Or	
	(b)	(i)	Sketch the circuit diagram of clamper and explain its operation.	(8)
		(ii)	Explain the operation of successive approximation A/D converter.	(8)
19.	(a)	the ope	umerate the desirable properties for a Voltage Controlled Oscillator (VCO). I circuit diagram of a Voltage Controlled Oscillator (VCO) and discusseration in a detailed manner with proper mathematical equation. umptions and approximations, if any.	
			Or	
	(b)	Dra	aw the block schematic diagram of PLL IC NE/SE 565and describe its function	tions. (16)
20.	(a)	Wi	th neat circuit diagram explain the operation of SMPS.	(16)
			Or	
	(b)	(i)	Describe the operation of isolation amplifiers.	(6)
		(ii)	Explain the operation of opto-coupler.	(10)