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Reg. No. : | | | | | | | | | | |

Question Paper Code: 53402

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2022

Third Semester

Electronics and Communication Engineering

15UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. In the eight input possibilities of a 3 input NOR gate, how many of those possibilities will effect in HIGH output? CO1- R

   (a) 1 (b) 2 (c) 4 (d) 8

2. A full adder can be constructed out of CO2- R

   (a) Two half adders (b) Two half adders and a OR gate

   (c) Two half adders and a NOT gate (d) Two half adders and a AND gate

3. The number of states a ring counter with 5 flip flops will have is CO3- R

   (a) 5 (b)10 (c) 32 (d) None of the above

4. In Moore models, output is function of only CO4- R

   (a) Present state (b) Input state (c) Next state (d) Both (A) and (B)

5. Transistor–transistor logic (TTL) is a class of digital circuits built from CO5- R

   (a) JFET (b) Resistors

   (c) Bipolar Junction Transistors (d) Bipolar Junction Transistors and Resistors

PART – B (5 x 3= 15Marks)

6. State the drawbacks of K-map method. CO1- R

7. Compare decoder and demultiplexer. CO2- R

8. Differentiate flip-flop from latches. CO3- R

9. Define hazards in asynchronous sequential circuits. CO4- R

10. What is the difference between programmable array logic (PAL) and programmable logic array (PLA)? CO5- R

PART – C (5 x 16= 80 Marks)

11. (a) Simplify the following Boolean function $f(W, X,Y,Z)=\sum m(2,6,8,9,10,11,14,15)$ using Quine-McClukey tabular method. CO1- App (16)

Or

(b) Find a minimal sum of products representation for $F(A,B,C,D) = \sum_m(1,3,7,11,15) + \sum d(0,2,5)$ using karnaugh method. Draw the circuit of the minimal expression using only NAND gates. CO1- App (16)

12. (a) Design a 4 bit magnitude comparator and draw its logic diagram. CO2- App (16)

Or

(b) Explain the design of BCD adder. CO2- App (16)

13. (a) (i) Draw the logic diagram of a 4-bit universal shift register and explain its operation. CO3- U (8)

(ii) Explain the working of a Master - slave J-K flip-flop with a neat logic Diagram. CO3- U (8)

Or

(b) Design and explain the working of synchronous MOD-6 counter. CO3- U (16)

14. (a) Design a sequence detector that produces an output '1' whenever the non-overlapping sequence 1011 is detected. CO4- U (16)

Or

(b) Explain in detail about problems in asynchronous sequential circuits. CO4- U (16)

15. (a) Implement the following two Boolean functions with a programmable logic array (PLA) CO5- U (16)

$F_1(A,B,C) =\sum m(0,1,3,4)$

$F2(A,B,C) =\sum m(1,2,3,4,5)$

Or

(b) (i) Discuss about FPGA in detail. CO5- U (8)

(ii) Explain the operation of a TTL 3-input NAND gate with a neat circuit diagram. CO5- U (8)