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Reg. No.:					

# **Question Paper Code: 96402**

## B.E. / B.Tech. DEGREE EXAMINATION, MAY 2022

## Sixth Semester

## Electronics and Communication Engineering

	1	9UEC602-	– VLSI DESIGN	N				
		(Regul	lation 2019)					
ation: Three hours	Maximum:	Maximum: 100 Marks						
	A	answer AL	L Questions					
	PAl	RT A - (5	x 1 = 5  Marks					
1is a language used to describe a digital system								
(a) Verilog	(b) c prog	gram	(c) c++ Progr	ram (d) Java P	rogram			
The following one is	the not the	mode of th	ne MOSFET tran	nsistor	CO1-U			
(a) Accumulation mo	ode		(b) depletio	(b) depletion mode				
(c) Inversion mode	ersion mode							
To estimate the delay	y of logic ga	tes, the an	alytical method	used is	CO1-U			
(a) RC delay model	b (d) none	of the above						
In CMOS logic circu	it the n-MO	S transisto	or acts as		CO1- U			
(a) Load (b) Pull	up network	(c) Pull	down network	(d) Not used in CN	MOS circuits			
is used	in logic des	ign of VL	SI		CO1- U			
(a) LIFO	(b) FIFO		(c) FILO	(d) LILO				
	PAF	RT - B (5	x 3= 15 Marks)					
. List out any few applications involved in using verilog HDL								
What is the need for design rules?								
8. Write the expression for the logical effort and parasitic delay of n input NOR								
9. List the methods to reduce dynamic power dissipation.								
0. Give the applications of high speed adders.								
	(a) Verilog  The following one is  (a) Accumulation mode  (c) Inversion mode  To estimate the delay  (a) RC delay model  In CMOS logic circul  (a) Load (b) Pull to is used  (a) LIFO  List out any few app.  What is the need for  Write the expression  List the methods to responsible to the second	A PAI  is a language used to desc.  (a) Verilog (b) c prog.  The following one is the not the rect.  (a) Accumulation mode  (c) Inversion mode  To estimate the delay of logic gar.  (a) RC delay model (b) π delay.  In CMOS logic circuit the n-MO.  (a) Load (b) Pull up network.  is used in logic desc.  (a) LIFO (b) FIFO.  PAF.  List out any few applications inv.  What is the need for design rules.  Write the expression for the logic.  List the methods to reduce dyname.	Answer AL  PART A - (5  is a language used to describe a dig  (a) Verilog (b) c program  The following one is the not the mode of the  (a) Accumulation mode  (c) Inversion mode  To estimate the delay of logic gates, the and  (a) RC delay model (b) π delay model  In CMOS logic circuit the n-MOS transisted  (a) Load (b) Pull up network (c) Pull  is used in logic design of VLS  (a) LIFO (b) FIFO  PART – B (5 states out any few applications involved in used to the logical effort at the logical effort at the methods to reduce dynamic power	Answer ALL Questions  PART A - (5 x 1 = 5 Marks)  is a language used to describe a digital system  (a) Verilog (b) c program (c) c++ Programing (a) Accumulation mode (b) depletion (c) Inversion mode (d) non inversion mode (d) non inversion mode (e) both a& In CMOS logic circuit the n-MOS transistor acts as (a) Load (b) Pull up network (c) Pull down network is used in logic design of VLSI  (a) LIFO (b) FIFO (c) FILO PART – B (5 x 3= 15 Marks)  List out any few applications involved in using verilog HD What is the need for design rules?  Write the expression for the logical effort and parasitic delations.	Answer ALL Questions  PART A - (5 x 1 = 5 Marks)  is a language used to describe a digital system  (a) Verilog (b) c program (c) c++ Program (d) Java P  The following one is the not the mode of the MOSFET transistor  (a) Accumulation mode (b) depletion mode  (c) Inversion mode (d) non inversion mode  To estimate the delay of logic gates, the analytical method used is  (a) RC delay model (b) \pi delay model (c) both a& b (d) none  In CMOS logic circuit the n-MOS transistor acts as  (a) Load (b) Pull up network (c) Pull down network (d) Not used in CM  is used in logic design of VLSI  (a) LIFO (b) FIFO (c) FILO (d) LILO  PART - B (5 x 3= 15 Marks)  List out any few applications involved in using verilog HDL  What is the need for design rules?  Write the expression for the logical effort and parasitic delay of n input NOR  List the methods to reduce dynamic power dissipation.			

### $PART - C (5 \times 16 = 80 \text{ Marks})$

11. (a) Design 8-3 priority encoder using structural and data flow CO2- App (16)description with neat block diagram (b) Explain the hierarchical modeling concept of Top- Bottom and CO1- U (16)Bottom – Top approach in Verilog HDL with neat example 12. (a) Analyze the different operating regions involved in DC CO2-Ana (16)characteristic and output voltage of CMOS inverter. (b) Analyze the different regions of drain to source current involved CO2- Ana (16)in ideal I-V characteristics. Analyze the static and dynamic power consumption in CMOS CO4- Ana 13. (a) (16)logic circuits Or (b) Analyze the various factors involved to design reliable CMOS CO4- Ana (16)chips. Analyze the power of CVSL and DVSL logic with examples. 14. (a) CO5- Ana (16)(b) Describe about the concept of timing issues and pipelining. CO1-U (16)Explain the concept of carry look ahead adder with neat diagram. 15. CO1-U (16)Or (b) Explain the concept of modified booth multiplier with a suitable CO1- U (16)example.