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Reg. No. : | | | | | | | | | | |

Question Paper Code: 96402

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2022

Sixth Semester

Electronics and Communication Engineering

19UEC602– VLSI DESIGN

(Regulation 2019)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. _____is a language used to describe a digital system CO1-U

   (a) Verilog (b) c program (c) c++ Program (d) Java Program

2. The following one is the not the mode of the MOSFET transistor CO1-U

   (a) Accumulation mode (b) depletion mode

   (c) Inversion mode (d) non inversion mode

3. To estimate the delay of logic gates, the analytical method used is CO1-U

   (a) RC delay model (b) π delay model (c) both a& b (d) none of the above

4. In CMOS logic circuit the n-MOS transistor acts as CO1- U

   (a) Load (b) Pull up network (c) Pull down network (d) Not used in CMOS circuits

5. _____is used in logic design of VLSI CO1- U

   (a) LIFO (b) FIFO (c) FILO (d) LILO

PART – B (5 x 3= 15 Marks)

6. List out any few applications involved in using verilog HDL CO1- U
7. What is the need for design rules? CO1- U
8. Write the expression for the logical effort and parasitic delay of n input NOR CO2-U
9. List the methods to reduce dynamic power dissipation. CO2-U
10. Give the applications of high speed adders. CO2-U

PART – C (5 x 16= 80 Marks)

11.	(a)	Design 8-3 priority encoder using structural and data flow description with neat block diagram	CO2- App	(16)
		Or		
	(b)	Explain the hierarchical modeling concept of Top- Bottom and Bottom –Top approach in Verilog HDL with neat example	CO1- U	(16)
12.	(a)	Analyze the different operating regions involved in DC characteristic and output voltage of CMOS inverter.	CO2-Ana	(16)
		Or		
	(b)	Analyze the different regions of drain to source current involved in ideal I-V characteristics.	CO2- Ana	(16)
13.	(a)	Analyze the static and dynamic power consumption in CMOS logic circuits	CO4- Ana	(16)
		Or		
	(b)	Analyze the various factors involved to design reliable CMOS chips.	CO4- Ana	(16)
14.	(a)	Analyze the power of CVSL and DVSL logic with examples.	CO5- Ana	(16)
		Or		
	(b)	Describe about the concept of timing issues and pipelining.	CO1- U	(16)
15.	(a)	Explain the concept of carry look ahead adder with neat diagram.	CO1- U	(16)
		Or		
	(b)	Explain the concept of modified booth multiplier with a suitable example.	CO1- U	(16)