Reg. No. : | | | | | | | | | | |

Question Paper Code: 36404

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2022

Sixth Semester

Electronics and Communication Engineering

01UEC604 - VLSI DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What is channel length modulation?
2. What is meant by interconnect? What the types are of interconnect?
3. How to compute the delay of CMOS circuits?
4. What is the fundamental goal in device modeling?
5. What is meant by transparent latch? Draw any two types of transparent latch and write its limitation.
6. State any two criteria for low power logic design.
7. What is the need for testing?
8. What is mean by logic verification?
9. Give the basic difference between tasks and functions.
10. What are bitwise operators in Verilog?

PART - B (5 x 16 = 80 Marks)

11. (a) Explain in detail about ideal I-V characteristics and non-ideal characteristics of MOSFET. (16)

Or

(b) Illustrate the DC transfer characteristics of a CMOS inverter. (16)

12. (a) (i) Explain the static and dynamic power dissipation in CMOS circuit with necessary diagram and expression. (10)

(ii) Give a brief account on design margin. (6)

Or

(b) What is a BSIM model? Give its versions with SPICE levels. Mention the features of BSIM model. (16)

13. (a) Compare the various logic circuit families. (16)

Or

(b) (i) Discuss about the conventional CMOS flip flops. (8)

(ii) Summarize the sequencing of dynamic circuits. (8)

14. (a) Explain the logic verification in various levels of abstraction. (16)

Or

(b) Explain the method of boundary scan test in detail. (16)

15. (a) Write a Verilog HDL code for

(i) 2:4 decoder (ii) Equality detector using gate level modelling. (16)

Or

(b) Explain behavioral and gate level modeling with suitable example. (16)