Question Paper Code: 94805A

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2021

Fourth Semester

Information Technology

19UIT405 - COMPUTER ORGANIZATION AND ARCHITECTURE

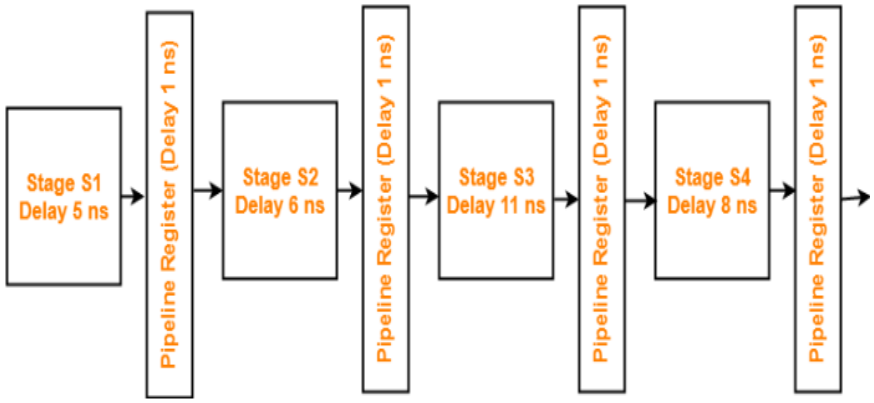
(Regulation 2019)

Duration: 1:45 hours Maximum: 50 Marks

Answer ALL Questions

PART A - (5 x 10 = 50 Marks)

1.	a.	An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (i) direct; (ii) immediate; (iii) relative (iv) register indirect; (v) index with R1 register as the index register.	Apply
		OR	
	b.	An instruction is stored at location 400 with its address field at location 301. The address field has the value 500. A processor register R1 contains the number 300. Evaluate the effective address if the addressing mode of the instruction is (i) direct; (ii) immediate; (iii) relative (iv) register indirect; (v) index with R1 register as the index register.	Apply
2.	a.	Multiply given signed 2's complement numbers using booth algorithm A=010111(Multiplicand) B=110110 (Multiplier).	Apply
		OR	
	b.	Multiply given signed 2's complement numbers using bit pair recoding A=110011 (Multiplicand) B=101100 (Multiplier)	Apply
3.	a.	Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate- 1. Pipeline cycle time 2. Non-pipeline execution time 3. Speed up ratio 4. Pipeline time for 1000 tasks 5. Sequential time for 1000 tasks 6. Throughput	Evaluate
		OR	

b.	Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure-  What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?	Evaluate
4. a.	Write the Flynn's classification with neat diagram.	Understand
	OR	
b.	Write the instruction level parallelism with neat diagram.	Understand
5.a.	Describe the data transfer method using DMA.	Understand
	OR	
b.	Express mapping schemes used in cache memory. (i) Direct (ii) Associate (iii) Set associate	Understand