Reg. No. : | | | | | | | | | | |

Question Paper Code: 33506

B.E. / B.Tech. DEGREE EXAMINATION, AUGUST 2021

Third Semester

Electronics and Instrumentation Engineering

01UEI306 – DIGITAL ELECTRONICS

(Regulation 2013)

Duration: 1:45 hour Maximum: 50 Marks

PART A - (10 x 2 = 20 Marks)

(Answer any ten of the following questions)

1. What is 8421 code?
2. State De-Morgan's theorem.
3. Draw the schematic of three input TTL NAND gate.
4. Suggest a solution to overcome the limitation on the speed of the adder.
5. Compute the excitation table of T flip flop.
6. Differentiate between edge triggering and level triggering.
7. Differentiate fundamental mode and pulse mode asynchronous sequential circuits.
8. What is race conditions?
9. Discriminate between PLA and PAL.
10. Compare EPROM with EEPROM.
11. Convert the octal number 360.15 to decimal number.
12. State De-Morgan's theorem.
13. Draw the schematic of three input TTL NAND gate.
14. Suggest a solution to overcome the limitation on the speed of the adder.

15. How a D flipflop is converted into T flipflop.

PART – B (3 x 10= 30 Marks)

(Answer any three of the following questions)

16. Compute the minimized Boolean expression using K-map
F = A'BC'D'+A'BC'D+ ABC'D'+ AB'C'D+ A'B'CD' (10)

17. Design a combinational logic using a suitable multiplexer to realize the Boolean expression: F = AD'+B'C+BC'D. (10)

18. Design a mod-7 synchronous binary counter using JK flip-flops. (10)

19. Design a asynchronous sequential circuit specified by the following flow table. (10)

	00	01	10	10
A	A.O	A.O	A.O	B.0
B	A,O	A.O	B.1	B.1

20. Implement the BCD to XS3 code conversion using ROM. (10)