Reg. No. : | | | | | | | | | | |

Question Paper Code: 43402

B.E. / B.Tech. DEGREE EXAMINATION, AUGUST 2021

Third Semester

Electronics and Communication Engineering

14UEC302 – DIGITAL ELECTRONICS AND DESIGN

(Regulation 2014)

Duration: 1:45 hour Maximum: 50 Marks

PART A - (10 x 2 = 20 Marks)

(Answer any ten of the following questions)

1. Use Boolean algebra to simplify the function $f = x(y + wz) + wxz$. Sketch the logic circuit for the minimized function using NAND gates.
2. Realize EX-OR Gate from NAND Gate.
3. Write the truth table for full subtractor.
4. Define decoder.
5. Differentiate the combinational logic from sequential logic.
6. What is meant by Shift Register? List its types.
7. State the advantages and disadvantages of TTL.
8. List the different types of memory.
9. What is the difference between synchronous and asynchronous sequential circuits?
10. Distinguish between static and dynamic hazards.
11. Obtain the *XS-3* code and 9's complement for $(428)_{10}$.
12. Find the complement of $A + BC + AB$.

13. Draw the logic diagram of a 4-bit adder- subtractor circuit.

14. What is data selector?

15. Mention the problems faced by ripple counter.

PART – B (3 x 10= 30 Marks)

(Answer any three of the following questions)

16. Realize the following function as Multilevel NAND –NAND gate and Multilevel NOR –NOR gate

$F = \overline{A}\,B + B\,(C + D) + E\overline{F}\,(\overline{B} + \overline{D})$ (10)

17. With logic diagram Truth table and explain about 3-to-8 decoder. (10)

18. With neat diagram explain in detail about how the race around condition is avoided in master-slave JK flip-flop. (10)

19. With block diagram explain about PLA and realize the following functions in PLA:

$F1 = \overline{A}\ B\ \overline{C} + A\ \overline{B}\ C + \overline{A}\ B\ C$

$F2 = A\ B + AC + \overline{A}BC$ (10)

20. Develop VHDL code for 3 to 8 decoder. (10)