Reg. No. : | | | | | | | | | | |

Question Paper Code: 33402

B.E. / B.Tech. DEGREE EXAMINATION, AUGUST 2021

Third Semester

Electronics and Communication Engineering

01UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2013)

Duration: 1:45 hour Maximum: 50 Marks

PART A - (10 x 2 = 20 Marks)

(Answer any ten of the following questions)

1. Obtain the canonical sum of product form of the function: $Y=AB + ACD$.
2. Draw the 4-bit binary divider.
3. Write the excitation table of RS flip-flop.
4. Draw the circuit diagram of a TTL-NAND gate with totem pole output.
5. List the design procedure of Asynchronous sequential circuits.
6. Define Associative law and Distributive law.
7. Compare half adder & full adder.
8. Differentiate between Latch and Flip-flop.
9. Draw the circuit diagram of a TTL-NAND gate with totem pole output.
10. List the design procedure of Asynchronous sequential circuits.
11. Implement 2 input Ex-OR gate using NAND gate.
12. With truth table draw the circuit of 3-bit odd parity generator.
13. State the drawbacks of RS flip flop.

14. How does a static RAM differ from dynamic RAM?

15. What arte advantages of merging process?

PART – B (3 x 10= 30 Marks)

(Answer any three of the following questions)

11. Simplify the following expression $F(w, x, y, z) = \sum_m (1, 3, 4, 5, 9, 10, 11) + \sum_d (6, 8)$ using Quine – McCluskey method. (10)

12. Implement the full subtractor using a 1: 8 demultiplexer. (10)

13. Discuss in detail about JK flip flop with its truth table, state diagram and characteristics equation. (10)

14. Implement the following two Boolean functions
F1(A,B,C) = ∑(0,1,2,4)
F2(A,B,C) = ∑(0,5,6,7) using
i) PLA ii) PAL iii) ROM (10)

15. Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change for any change in X. Use SR latch for implementation of the circuit. (10)