Reg. No. : | | | | | | | | | | |

Question Paper Code: 46404

B.E. / B.Tech. DEGREE EXAMINATION, AUGUST 2021

Sixth Semester

Electronics and Communication Engineering

14UEC604-VLSI DESIGN

(Regulation 2014)

Duration: 1:45 hour Maximum: 50 Marks

PART A - (10 x 2 = 20 Marks)

(Answer any ten of the following questions)

1. What is the objective of Layout rules?
2. List the various issues in Technology-CAD.
3. What is meant by crosstalk?
4. State the types of power dissipation.
5. Differentiate latch and flip-flop.
6. State any two criteria for low power logic design.
7. Name the different types of CMOS testing techniques.
8. What is mean by logic verification?
9. Write a verilog module for a half adder.
10. What are gate primitives?
11. Define body effect.
12. Give the types of design rules.

13. State the types of power dissipation.

14. List the different types of scaling.

15. Design a one transistor DRAM cell.

PART – B (3 x 10= 30 Marks)

(Answer any three of the following questions)

16. Explain layout design rules in detail. (10)

17. Explain in detail about delay estimation, logical effort and transistor sizing with example. (10)

18. Explain in detail: (i) Conventional CMOS Latch (ii) Conventional CMOS Flip flop. (10)

19 What are the various testing methods to be considered while designing a VLSI circuit? (10)

20. Explain the concept involved in structural gate level modeling and also give the description for Decoder and parity encoder. (10)