Reg. No. : | | | | | | | | | | |

Question Paper Code: 56424

B.E. / B.Tech. DEGREE EXAMINATION, AUGUST 2021

Sixth Semester

Electrical and Electronics Engineering

01UEC624 - APPLIED DIGITAL SIGNAL PROCESSING

(Common to EIE and ICE)

(Regulation 2013)

Duration: 1:45 hour Maximum: 50 Marks

PART A - (10 x 2 = 20 Marks)

(Answer any ten of the following questions)

1. Compare deterministic and random signals.
2. Show that the discrete time system described by the input-output relationship $y(n) = nx(n)$ is linear?
3. Summarize three methods of doing inverse Z-transform.
4. Deduce the convolution sum of two sequences of $x(n) = \{3, 2, 1, 2\}$ and $h(n) = \{1, 2, 1, 2\}$.
5. Express the 2-point radix-2 DIT-FFT butterfly structure for DFT. What is its advantage?
6. Define twiddle factor of FFT.
7. Give the steps in the design of a digital filter from analog filter.
8. Distinguish between FIR filters and IIR filters.
9. Illustrate the block diagram of Modified Harvard architecture.
10. Mention various stages in pipelining.
11. List out the applications of digital signal processing.
12. What is aliasing? How can it be eliminated?
13. State the scaling property of the Z transforms.

14. Define discrete Fourier series.

15. Determine the DFT of the sequence *x(n) = {1, 1, -2, -2}.*

PART – B (3 x 10= 30 Marks)

(Answer any three of the following questions)

16. Explain the process of reconstruction of the signal from its samples with expression. (10)

17. Discover the general solution of the difference equation $y(n) = x(n) - 3y(n-1)$ with initial condition $y(-1) = 0$ and input $x(n) = n^2 + n$. (10)

18. Compute the eight-point DFT of the sequence$x(n) = \{n + 1\}$, Using the radix-2 decimation-in-time algorithm. (10)

19. Design a low pass filter using rectangular window by taking 9 samples of *W(n)* and with a cutoff frequency of 1.2 *rad /sec*. (10)

20 Explain the architecture of TMS320C50 with a neat diagram. (10)