Reg. No. : | | | | | | | | | | |

Question Paper Code: 36404

B.E. / B.Tech. DEGREE EXAMINATION, AUGUST 2021

Sixth Semester

Electronics and Communication Engineering

01UEC604 - VLSI DESIGN

(Regulation 2013)

Duration: 1:45 hour Maximum: 50 Marks

PART A - (10 x 2 = 20 Marks)

(Answer any ten of the following questions)

1. What is the objective of Layout rules?
2. List the various issues in Technology-CAD.
3. What is meant by crosstalk?
4. State the types of power dissipation.
5. Differentiate latch and flip-flop.
6. State any two criteria for low power logic design.
7. Name the different types of CMOS testing techniques.
8. What is mean by logic verification?
9. Write a verilog module for a half adder.
10. What are gate primitives?
11. What is the purpose of design rule?
12. Define twin – well process? Why it is so called?

13. State the types of power dissipation.

14. What is meant by design margin?

15. State the reasons for the speed advantage of CVSL family.

PART – B (3 x 10= 30 Marks)

(Answer any three of the following questions)

16. Explain in detail about ideal I-V characteristics and non-ideal characteristics of MOSFET. (10)

17. Explain the static and dynamic power dissipation in CMOS circuit with necessary diagram and expression. (10)

18. Compare the various logic circuit families. (10)

19. Explain the logic verification in various levels of abstraction. (10)

20. Write a Verilog HDL code for

    (i) 2:4 decoder (10)