Reg. No. : | | | | | | | | | | | | |

Question Paper Code:R2I04

B.E./B.Tech. DEGREE EXAMINATION, APRIL / MAY 2025

Second Semester

CSE (Internet of Things)

R21UIO204- DIGITAL SYSTEM DESIGN

(Regulations R2021)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1.	State De-Morgan's theorem.	CO1- U
2.	Express the function Y = A+ BC in canonical POS.	CO2-App
3.	Why full adder is efficient than the half adders? Justify.	CO3-Ana
4.	Determine the Boolean expression for a half adder.	CO2-App
5.	Write the characteristics table of a D flip flop.	CO1- U
6.	The clock frequency is 2MHz. How long will it take to serial load the eight shift register?	CO2-App
7.	How can a race in digital circuits can be avoided?	CO2-App
8.	What is the most important consideration in making state assignments for asynchronous network?	CO1- U
9.	How does the architecture of a PAL differ from a PROM?	CO3-Ana
10.	Define Cache memory.	CO1- U

PART – B (5 x 16= 80 Marks)

11. (a) For the given truth table ,write the logical expression in the canonical SOP & POS CO2- App (16)

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Or

(b) Write the minimized Boolean expression for the function using K-map — CO2- App — (16)

F (w,x,y,z)= ∑m(0,1,2,4,5,6,8,9,12,13,14).

12. (a) Write a brief note on the following combinational circuits: — CO1- U — (8)

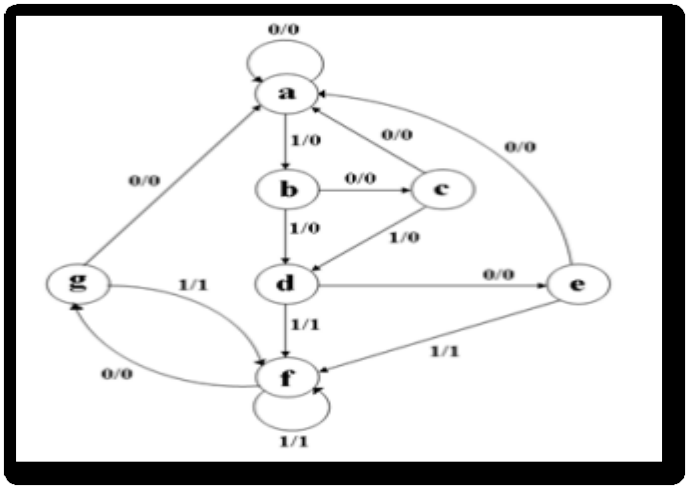
(i) Full adder

(ii) Full subtractor — CO1- U — (8)

Or

(b) Explain in detail the BCD Adder. — CO1- U — (16)

13. (a) Analyze state reduction if possible after designing a clocked synchronous sequential logic circuit using JK flip flops for the following state diagram. Use state reduction if possible. — CO2- App — (16)



Or

(b) Design a synchronous counter using JK flipflops to count the sequence 0,1,2,4,5,6,0,1,2.Use State diagram and state table. — CO2- App — (16)

14. (a) Write a HDL structural description of a full adder using two half adder and OR Write the simulation waveform — CO2- App — (16)

Or

(b) An asynchronous sequential circuit is described by the following excitation and output function: $Y = X_1X_2 + (X_1 + X_2)Y$, — CO2- App — (8)

$$Z = Y$$

(i) Draw the logic diagram of the circuit

(ii) Derive the transition table, output map and describe the behavior of the circuit — CO2- App — (8)

15. (a) Differentiate static and dynamic RAM. Draw the circuits of one cell of each and explain its working principle. CO1- U (16)

Or

(b) Write a detailed notes on : CO1- U (8)

(i) PAL

(ii) FPGA CO1- U (8)