C **Reg. No. :** | | | | | | | | | | | | |

Question Paper Code: U6402

B.E. / B.Tech. DEGREE EXAMINATION, APRIL / MAY 2025

Sixth Semester

Electronics and Communication Engineering

21UEC602- VLSI DESIGN

(Regulations 2021)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. _____is a language used to describe a digital system CO1-U

   (a) Verilog (b) c program (c) C++ Program (d) Java Program

2. The distance between the source and drain is called CO1-U

   (a) Channel (b) Gate (c) Drain (d) Source

3. The resistance and capacitance product of the MOS transistor is called CO1-U

   (a) intrinsic delay (b) Extrinsic delay (c) both (a) & (b) (d) none of the above

4. Physical and electrical specification is given in____ CO1-U

   (a) architectural design (b) logic design (c) system design (d) functional design

5. High and low noise margins can be equalized by CO1-U

   (a) βn = βp (b) βn greater than βp (c) βn lesser than βp (d) Lp = 2Ln

PART – B (5 x 3= 15 Marks)

6. Design a D flip-flop circuit using behavioral level description. CO2 - App

7. Sketch a 3 input NAND gate with transistor widths chosen to achieve effective rise and fall resistance equal to that of a unit inverter(R). CO3 - App

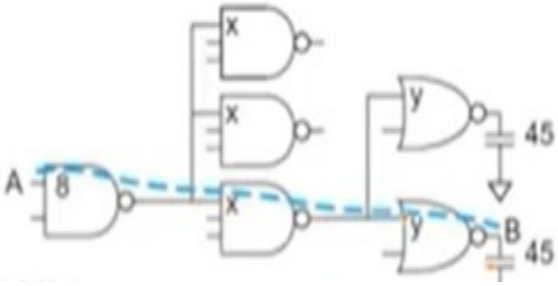
8. Define power dissipation. CO1 – U

9. Design the AND gate using pseudo NMOS logic. CO3- App

10. What is Low Power Logic Styles? CO1 – U

PART – C (5 x 16= 80 Marks)

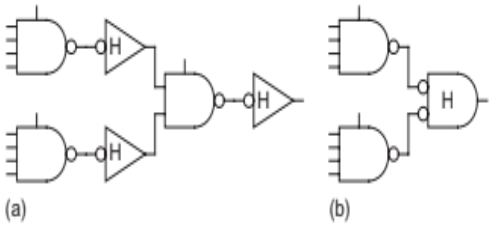
11.	(a)	(i) Design 4 bit input device and write a Verilog code for following conditions, it combines 4 bit at a time as a single output according to the selection line inputs.	CO2-App	(8)
		(ii) Write a Verilog program for 3 to 8 decoder in gate level description.	CO2-App	(8)
		Or		
	(b)	Design a 4-bit adder in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder using Verilog HDL.	CO2-App	(16)
12.	(a)	Explain the n- well process in CMOS fabrication.	CO1 – U	(16)
		Or		
	(b)	Explain the basic structure and operating mode of N- MOS Transistor based on the magnitude of Vgs.	CO1 – U	(16)
13.	(a)	Estimate the minimum delay of the path from A to B in the given Figure and choose transistor sizes to achieve this delay. The initial NAND gate may present a load of 8λ of transistor width on the input and the output load is equivalent to 45λ of transistor width. How should be the transistors be sized to achieve least delay?.	CO3-App	(16)



Or

	(b)	Determine the relative saturation current of 2- and 3-transistor nMOS and pMOS stacks in a 65 nm process. VDD = 1.0 V and Vt = 0.3 V. Use Vc = Ec L = 1.04 V for nMOS devices and 2.22 V for pMOS devices.	CO3-App	(16)

14. (a) Two designs for an 8-input domino AND gate using footed dynamic gates are shown in Figure. One uses four stages of logic with static CMOS inverters. The other uses only two stages by employing a HI-skew NOR gate. Analyze at what range of path electrical efforts are the 2-stage design faster? CO5-Ana (16)



Or

(b) A Multiplexer has a maximum input capacitance of 16 units on each input it must drive load of 150 units analyze the minimum delay for NAND and Compound solution. CO5-Ana (16)

15. (a) Explain in detail about variable threshold voltage and multiple threshold voltage is infeasible due to technological limitation necessary diagrams. CO1 – U (16)

Or

(b) Explain the need and demand of low power CMOS logic circuits CO1 – U (16)