C **Reg. No. :** | | | | | | | | | | | | |

Question Paper Code: R2205

B.E. / B.Tech. DEGREE EXAMINATION, APRIL / MAY 2025

Second Semester

Computer Science and Engineering

R21UCS205- DIGITAL ELECTRONICS

(Common to CSE(SC) Engineering branches)

(Regulations R2021)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5Marks)

1. Binary addition 0+1 is equal to_____ CO2-App

   (a) 1 (b) 0 (c) 2 (d) 3

2. Infer the Boolean expression of borrow in half-subtractor CO1-U

   (a) AB' (b) A'B (c) AB (d) A'B'

3. In the case of a J-K flip-flop with active _____inputs, the output of the flip-flop toggles CO1-U

   (a) High (b) Low (c) Half (d) Partials

4. In Asynchronous circuit , the changes occur with the change of____ CO1-U

   (a) input (b) output (c) clock pulse (d) time

5. A table specifying the fuse map of a PLA is called _____ CO1-U

   (a) fuse table (b) fuse map table (c) programming table (d) PLA table

PART – B (5 x 3= 15 Marks)

6. Find the 2's complement of following binary value 10111011 CO2-App
7. Define combinational logic. CO1-U
8. What are the different types of flip-flop? CO1-U
9. State the problems in Asynchronous Sequential Circuits CO1-U
10. What is programmable logic array? How it differs from ROM? CO1-U

PART – C (5 x 16= 80 Marks)

11.	(a)	Solve the following: (i) $(1001010.1101001)_2$ to $base_{10}$ (ii) $(15.32)_{10}$ to $base_2$ (iii) $(1011DA)_{16}$ to $base_{10}$	CO2-App	(16)
		Or		
	(b)	Plot the following Boolean function in Karnaugh map and simplify it in SOP $F(W,X,Y,Z) = \sum (7,9,10,11,12,13,14,15)$	CO2-App	(16)
12.	(a)	Design Full Adder and derive expression for Sum and Carry in Cin(X,y) with circuit diagram.	CO2-App	(16)
		Or		
	(b)	Design a logic circuit that accepts a 4-bit Gray code and converts it to 4bit Binary code with input (G3,G2,G1,G0) and output (B3,B2,B1,B0)?	CO2-App	(16)
13.	(a)	Derive the operation of D and T flip-flops and answer the following (i) Draw the logic diagram of the circuit. (ii) Derive the Truth table. (iii) Derive Excitation Table (iv) Derive State Diagram	CO1-U	(16)
		Or		
	(b)	Explain the following Shift Registers in detail (a) SIPO (b) PISO (c) PIPO	CO1-U	(16)
14.	(a)	Design an asynchronous sequential circuit with two inputs X1,X2 and one output Initially both inputs are equal to 0.when X1 or X2 becomes 1output becomes 1.when second input also becomes 1output changes to 0.the output stays at 0 until the circuit goes back to initial state.	CO2-App	(16)
		Or		
	(b)	Design of Hazard free switching circuits for static,dynamic and essential hazards	CO2-App	(16)
15.	(a)	Explain in detail about the classification of memories with neat block diagram?	CO1-U	(16)
		Or		
	(b)	Explain the Characteristic function of RTL and ECL circuits in Logic families.	CO1-U	(16)

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