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Question Paper Code:R2E05

B.E./B.Tech. DEGREE EXAMINATION, APRIL / MAY 2025

Second Semester

Artificial Intelligence and Data Science

R21UAD205- DIGITAL LOGIC AND DESIGN

(Regulations R2021)

(Common to CSE(AIML) Engineering branches)

Duration: Three hours

Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

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| 1. Find 2's complement: 1101110101 | CO2-App |
| 2. To Perform BCD Addition for given number: 788 and 879 | CO2-App |
| 3. Define half adder and full adder | CO1- U |
| 4. Write down the applications of Multiplexer | CO1- U |
| 5. Derive the characteristic equation of a D flip flop. | CO1- U |
| 6. Explain D flip-flop | CO1- U |
| 7. What are the types of hazards? | CO1- U |
| 8. What is the need of state reduction in sequential circuit design? | CO1- U |
| 9. Define ROM | CO1- U |
| 10. Explain PLA | CO1- U |

PART – B (5 x 16= 80 Marks)

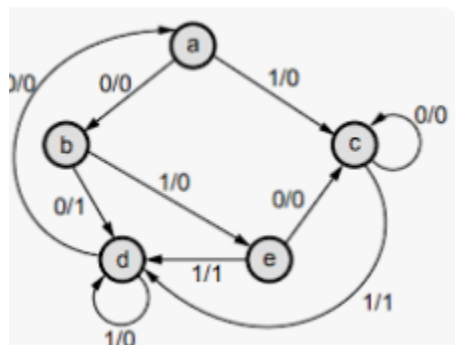
11. (a) Reduce the following 4 variable function to its minimum sum of products form: CO2-App (16)
- $$Y = \overline{A}\overline{B}\overline{C}D + \overline{A}B\overline{C}D + \overline{A}BCD + \overline{A}BC\overline{D} + A\overline{B}\overline{C}D + A\overline{B}C\overline{D} + ABCD + A\overline{B}CD$$
- Or
- (b) Simplify the Boolean expression by using a QuineMcCluskey method CO2-App (16)
- $$F(A,B,C,D) = \sum m(0,2,3,6,7,8,10,12,13)$$

12. (a) (i) Differentiate between half adder and full adder? CO1- U (8)
(ii) With an aid of block diagram clearly distinguish between a decoder and encoder. CO1- U (8)

Or

- (b) What is decoder? Draw the block diagram and truth table for 2 to 4 decoder. CO1- U (16)
13. (a) Design a synchronous counter to count in the following Sequences 0,1,2,3,4,5,6, Using JK flip flop. CO2-App (16)
- Or
- (b) Using SR flip flops, design a parallel counter which counts in the sequence 000,111,101,110,001,010,000 CO2-App (16)
14. (a) Design an asynchronous sequential circuit with inputs x_1 and x_2 and one output z . Initially and at any time if both the inputs are 1, output is equal to 0. When x_1 or x_2 becomes 1, z becomes 1. When second input also becomes 0, $z=1$ the output stays at 1 until circuit goes back to initial state CO2-App (16)

- (b) Design a sequential circuit involves the representation of sequential circuit models. It includes a state diagram, state table, reduced state table CO2-App (16)



15. (a) Explain in detail about Error correction with an example ? CO1- U (16)
- Or
- (b) Explain in detail about Static and dynamic ROM with neat diagram? CO1- U (16)