A **Reg. No. :** | | | | | | | | | | | | |

Question Paper Code: U4303

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2024

Fourth Semester

Electrical and Electronics Engineering

21UEE403-PRINCIPLES OF DIGITAL ELECTRONICS

(Regulations 2021)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. How many entries will be in the truth table of a 4-input NAND gate? CO1- U

(a) 4 (b) 8 (c) 16 (d) 32

2. Identify the even parity code from the following CO1- U

(a) 11001 (b) 1110 (c) 0111 (d) 0110

3. What will be the number of selection lines in a 16 to 1 Multiplexer? CO1- U

(a) 2 (b) 3 (c) 4 (d) 5

4. Which pair of Boolean expressions satisfies the idempotency property? CO1- U

(a) $A+\overline{A}=1$, $A.\overline{A}=0$ (b) A+A=A, A . A=A

(c) A + 1 = 1, A . 1 = A (d) A + 0 = A, A . 0 = 0

5. Find the output of SR flip flop when S=1, R=0 is? CO1- U

(a) 1 (b) 0 (a) 1 (b) 0

6. Find the output of D Flipflop when D=1? CO1- U

(a) 1 (b) 0 (a) 1 (b) 0

7. How many natural states will there be in a 4-bit ripple counter? CO1-U

(a) 4 (b) 8 (c) 16 (d) 32

8. Internal propagation delay of asynchronous counter is removed by CO1- U

(a) Ripple counter (b) Ring counter (c) Modulus counter (d) Synchronous counter

9. The Verilog HDL code starts with the keyword CO1- U

(a) always (b) module (c) end module (d) items

10. Which of the following loops are supported by verilog? CO1- U

(a) if-else loop (b) for loop

(c) while loop (d) All the above

PART – B (5 x 2= 10 Marks)

11. Classify the types of Binary Codes based on positional weighting CO1- U

12. Explain SOP and POS. CO1- U

13. Describe sequential logic circuit. Give an example. CO1- U

14. Explain the various types of Hazards in sequential circuits. CO1- U

15. Write Verilog code to realize EXOR function. CO2- AP

PART – C (5 x 16= 80 Marks)

16. (a) Explain the types of weighted and non-weighted codes with an example for each type. CO1- U (16)

Or

(b) Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction (a) X-Y and (b) Y-X using 2's Complement and also using 1's Complement. CO1- U (16)

17. (a) (i) Simplify the following function using K-Map. CO2- App (16)

$F(A,B,C,D)= \sum m(0,1,2,3,4,6,8,9,10,12,14,15)$.

(ii) Design a half subtractor and implement using logic gates.

Or

(b) (i) Simplify the following function using K - Map and implement using gates. CO2- App (16)

$F(PQ,R,S) = \sum m(0,1,2,4,7,10,11,12)$

(ii) Design a full adder and implement using logic gates.

18. (a) Design synchronous sequential circuit that goes through the count sequence 1,3,4,5 repeatedly. Use T flip-flops for your design. CO2- App (16)

Or

(b) Design a synchronous Modulo-5 Up Counter using JK flip-flops CO2- App (16)

19. (a) Develop a PLA circuit to implement the logic function A'BC+AB'C+AC' and A'B'C'+BC — CO3- App — (16)

Or

(b) Implement the following function using PLA — CO3- App — (16)
F1 (A, B, C) = Σ(1, 2, 4, 6);
F2 (A, B, C) = Σm(0, 1, 6, 7);
F3 (A, B, C) = Σ(2,6).

20. (a) Develop Verilog code for full adder using gate level and data flow modeling. — CO3- App — (16)

Or

(b) Write Verilog code to design 3 to 8 decoder using gate level and behavioural modeling. — CO3- App — (16)