C

Reg. No. : | | | | | | | | | | | | |

Question Paper Code: 95602

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2024

Sixth Semester

Electronics and Communication Engineering

21UEC602 - VLSI DESIGN

(Regulations 2021)

Duration: Three hours | Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5Marks)

1. In a verilog code, the module declaration consists of____ CO1- U

   (a)Wire (b) inputs (c) gates (d) I/O ports

2. In the cutoff region of the transistor , the current flow CO1- U

   (a) zero (b) constant (c) variable (d) None of the above

3. To estimate the delay of logic gates, the analytical method used is CO1- U

   (a) RC delay model (b) π delay model (c) both (a) & (b) (d) None of the above

4. What is the delay required to perform a single operation in a pipelined structure? CO1- U

   (a) 2n (b) 3n (c) 4n (d) n

5. α is used for scaling CO1- U

   (a) linear dimensions (b) v_{dd} (c) oxide thickness (d) non linear

PART – B (5 x 3= 15Marks)

6. List out the conditional statements in Verilog HDL. CO1 -U
7. Compare N-MOS and P-MOS Transistor. CO1- U
8. Define power dissipation. CO1 – U
9. Design an AND gate using pass transistor. CO3 - App
10. What is Low Power Logic Styles? CO1 – U

PART – C (5 x 16= 80Marks)

11.	(a)	Explain the VLSI design flow of Verilog HDL.	CO1 – U	(16)
		Or		
	(b)	Explain the design hierarchy of Verilog HDL with neat example.	CO1 – U	(16)
12.	(a)	Design the OUT=(AB+CD)' using CMOS layout design rules.	CO3 –App	(16)
		Or		
	(b)	Draw the Stick diagram and layout diagram for 2 input NAND and 2 input NOR gate.	CO3 –App	(16)
13.	(a)	Discuss the principle of constant field scaling and also write its effect on device characteristics.	CO1 – U	(16)
		Or		
	(b)	Discuss the different reliability problems related to the design of reliable chips.	CO1 – U	(16)
14.	(a)	Explain the sequencing methods of sequential static circuits.	CO1 – U	(16)
		Or		
	(b)	Explain the concept of modified booth multiplier with suitable examples.	CO1 – U	(16)
15.	(a)	Analyze the Different voltage scaling method using to design low power CMOS Circuits.	CO5 – Ana	(16)
		Or		
	(b)	Analyze different voltage scaling methods for low power design influence of voltage scaling on power and delay.	CO5 – Ana	(16)