С		Reg. No. :											
Question Paper Code: R2205													
B.E./B.Tech. DEGREE EXAMINATION, MAY 2024													
Second Semester													
Computer Science and Engineering													
R21UCS205- DIGITAL ELECTRONICS													
(Common to Cyber Security Engineering branch)													
(Regulations R2021)													
Dura	ation: Three hours	Maxim							imur	um: 100 Marks			
Allswei All Questions $PART A = (5x \ 1 - 5 Marks)$													
1.	Binary addition 0+1 is equal to											CC)1- U
	(a) 1	(b) 0		(c) 2						(d) 3			
2.	The Full adder is a	ne Full adder is a input and output combinational Circuit								CO1- U			
	a)2 and 1	(b) 2 and 2		(c)3 and 3						(d) 3 and 2			
3.	When both inputs of a J-K flip-flop cycle, the output will											CC)1- U
	(a) Be invalid	Be invalid (b) Change (c) Not change								(d) Toggle			
4.	The complexity of the	complexity of the asynchronous circuit is involved in timing								CO1- U			
	problems of												
	(a) inputs	(b) Latches		(c) fe	edba	ck pa	ath			(d) c]	lock	puls	es
5.	Which type of device I	/hich type of device FPGA are?										CC)1- U
	(a) SLD	SLD (b) SROM (c) EPROM							(d) PLD				
_		PART –	- B (5 x	3=15	Mark	cs)							
6.	What is Boolean algeb	ra?										CO	i - U
7.	Define Half adder and write its Truth table										CO	l - U	
8.	What is the application table of a D flip-flop?										CO	l - U	
9.	What is hazard?											CO:	l- U
10.	Define PROM.											CO	I - U

- $PART C (5 \times 16 = 80 Marks)$ 11. (a) Solve the following: CO2 - App (16)(i) $(1001010.1101001)_2$ to base10 (ii) $(12.32)_{10}$ to base2 (iii) $(101FA)_{16}$ to base10 Or (b) Plot the following Boolean function in Karnaugh map and CO2 - App (16)simplify it in SOP $F(w,x,y,z) = \sum (7,9,10,11,12,13,14,15)$ Design Full subtractor and derive expression for difference and CO2- App 12. (a) (16)borrow. Cin(X,Y) with circuit diagram. Or (b) Design Full Adder and derive expression for Sum and Carry in CO2- App (16)Cin(X,y) with circuit diagram. 13. (a) Design of 4 bit Ring counter with the help of state diagram, state CO2- App (16)
 - table, Excitation table and maps.

Or

- (b) Design of Ripple counter with the help of logic diagram and truth CO2- App (16) table.
- 14. (a) Why Hazards may happens in the asynchronous sequential CO1- U (16) circuits and discuss how to avoid Hazards ?

Or

- (b) Explain in detail about races with suitable example? CO1- U (16)
- 15. (a) Explain the Characteristic function of RTL and ECL circuits in CO1-U (16) Logic families.

Or

(b) Discuss in detail about Programmable Logic Devices With the help CO1-U (16) of its block diagram.