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Question Paper Code : 95302

5 Year M.Sc. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Fourth Semester

Software Engineering

ESE 042 — OPERATING SYSTEM AND SYSTEM SOFTWARE

(Regulations 2010)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Distinguish between assembler and interpreter.
2. Write any two basic macro processor functions.
3. Describe the actions taken by a kernel to context-switch between processes.
4. Differentiate hard real system and soft real system.
5. Define short term scheduler.
6. Define race condition.
7. What is the difference between page and a page frame?
8. What is a page fault?
9. List the various file attributes.
10. What is meant by virtual memory? Give some major benefits which are make applicable.

PART B — (5 × 16 = 80 marks)

11. (a) Write short notes on
 - (i) Design of a macro pre processor. (8)
 - (ii) Conditional macro expansion. (8)
- Or
- (b) Explain in detail about the pass structure of assembler and two pass assembler. (16)

12. (a) (i) Write detailed explanation about Multiprocessor scheduling and Real time scheduling. (10)
(ii) Give a brief note on mainframe systems. (6)

Or

- (b) (i) Explain the various synchronization mechanisms available to provide inter process coordination and communication. (8)
(ii) List out the various process states and briefly explain with a state diagram. (8)
13. (a) (i) What are semaphores? Explain their usage, implementation given to avoid busy waiting and binary semaphores. (10)
(ii) What is the use of monitors for resource allocation? (6)

Or

- (b) Consider the following set of processes, with the length of CPU-burst time given in millisecond.

Process	Burst time	Priority
p1	10	3
p2	1	1
p3	2	3
p4	1	4
p5	5	2

The processes are assumed to have arrived in order p1, p2, p3, p4, p5 all at time 0.

- (i) Draw Gantt charts illustrating the execution of these processes using FCFS, SJF, a non-preemptive priority (a smaller priority number implied a higher priority) and RR (quantum=1) scheduling.
(ii) What is the turnaround time of each process for each of the scheduling algorithms in part (i)? (16)
14. (a) Explain the advantages and disadvantages of segmented and paged implementation of virtual memory. Explain through a diagram, the principles of address translation in combined segmentation and paging. What is the drawback of this translation scheme? (16)

Or

- (b) (i) Explain about the methods used to prevent deadlocks. (8)
(ii) How does a deadlock can be avoided using Banker's algorithm? (8)

15. (a) (i) Give an overview of the various protection and access control mechanisms implemented in a file system. (8)
- (ii) How does the system detect thrashing? Once it detects thrashing what the system do to eliminate this problem? (8)

Or-

- (b) (i) Explain any two page replacement algorithms. (8)
- (ii) Explain the concept of demand paging and the performance issue of demand paging. (8)
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