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Question Paper Code : 95380

5 Year M.Sc. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

First Semester

Software Engineering

XCS 114/10677 SW 104 — DIGITAL PRINCIPLES

(Common to 5 Year M.Sc. Information Technology and M.Sc. Computer Technology)

(Regulation 2003/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Using 10's complement, subtract 3250 from 72532.

2. And $(1230)_4$ and $(23)_4$ without converting to decimal.

3. Write the general syntax for entity declaration in VHDL.

4. Realize OR logic function using 2 : 1 multiplexer.

5. Write D-Morgans theorems.

6. Differentiate between combinational logic circuit and sequential logic circuit.

7. What are the general capabilities of the shift register?

8. What are the differences between ring counter and Johnson counter?

9. What are hazards classed as undesirable for feedback variables?

10. Define clock skew.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Draw the logic circuit for the expression

$$F(A,B,C)=[AB'(C+BD)+A'B]C$$

Simplify the expression then draw the logic circuit for the simplified expression. (8)

(ii) State and prove De-Morgan's theorems. (8)

Or

(b) (i) Express the following in sum of minterms and product of maxterms

(1) $F(A,B,C)=(A'+B))B'+C)$ (5)

(2) $F(X,Y,Z)=(XY+Z)(Y+XZ)$. (5)

(ii) Convert the following to the other canonical form

(1) $F(A,B,C,D)=\Sigma m(1,3,7)$. (3)

(2) $F(X,Y,Z)=\pi(0,3,6,7)$. (3)

12. (a) Design and implement and 8-bit magnitude comparator. (16)

Or

(b) (i) Implement a full substractor with two half-subtractor and an OR gate. (8)

(ii) Design a combinational circuit that accepts a three bit number and generates an output binary number equal to the square of the input number. (8)

13. (a) A sequential circuit has two flip flops (A and B) two inputs (x and y) and an output (z). The flip flop input functions and the circuit output function are as follows :

$J_A = xB + y'B'$ $\quad K_A = xy'B'$

$J_B = xA'$ $\quad K_B = xy' + A$

$z = xyA + x'y'B$

Obtain the logic diagram, state diagram and state equation. (16)

Or

(b) (i) Design a counter with the following binary sequence 0, 4, 2, 1, 6 and repeat. Use JK flip flops. (8)

(ii) Explain state assignment and state reduction using suitable example. (8)

14. (a) (i) Draw the circuit diagram of a **bidirectional** shift register with parallel load facility and explain its **working.** (11)

(ii) Design a mod 6 counter. (5)

Or

(b) (i) Design a 3 bit Johnson counter using JK flip flops. (10)

(ii) Discuss the different types of ROM in brief. (6)

15. (a) An asynchronous sequential circuit has two internal states and one output. The excitation and output function describing the circuit are :

$$Y_1 = x_1x_2 + x_1y_2' + x_2'y_1$$
$$Y_2 = x_2 + x_1y_1'y_2 + x_1'y_1$$
$$z = x_2 + y_1$$

(i) Derive the transition table and output map. (6)

(ii) Obtain the flow table for the circuit. (6)

(iii) Draw the logic diagram of the circuit. (4)

Or

(b) (i) Obtain a binary state assignment for the reduced flow table shown in Figure 15 (b) (i). Avoid critical race conditions. (8)

	x_1, x_2 00	01	11	10
a	(a),0	(a),1	b,–	d,–
b	a,–	(b),0	(b),0	c,–
c	a,–	–,–	d,–	(c),0
d	a,–	a,–	(d),1	(d),1

Fig 15 (b) (i)

(ii) Obtain the logic diagram of the circuit using NAND latches and gates. (8)