LIB
7/1/16 FN

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M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Elective

Applied Electronics

VL 9261/AP 954/UAP 9167/10244 VLE 11 — ASIC DESIGN

(Common to M.E. Computer and Communication and M.E. VLSI Design/
M.E. Electronics and Communication Engineering)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the types of ASIC.

2. Define logical effort.

3. What are the features of metal – metal antifuse?

4. What is meant by metastability?

5. What is a meander factor?

6. State the advantages of Altera MAX 5000 interconnect.

7. Define the following terms in VHDL :

   (a) Delta time

   (b) Delta delay.

8. What is the purpose of ATPG?

9. List any four issues that are to be considered when partitioning a complex system into custom ASICs.

10. Name the goals and objectives of detailed routing.

PART B — (5 × 16 = 80 marks)

11. (a) (i) With the schematic, explain the steps involved in VLSI design flow. (10)

(ii) The chip size of a CPU is 25 mm × 25 mm with clock frequency of 100 mHz operating at 1.5 v. The length of the clock routing is estimated to be double the circumference of the chip. Assume that the clock signal is routed on a metal layer with width of 1.5 μm and the parasitic capacitance of the metal layer is 1 pf / μm^2. What is the power dissipation of the clock signal? (6)

Or

(b) (i) Discuss the data path logic cell with an example. (6)

(ii) What is a transmission gate? Explain how a multiplexer can be formed using transmission gate. (6)

(iii) Realize the following Boolean function using CMOS logic $Y = \overline{A + B}$. (4)

12. (a) (i) With a neat sketch, explain the programming of Antifuse. What are its advantages and disadvantages? (8)

(ii) Discuss the bench mark circuits proposed by PREP for the selection of programmable ASICs. (8)

Or

(b) (i) Draw and explain the features of XILINX 3000 CLB and the different types of interconnections. (10)

(ii) Discuss the various AC and DC issues common to FPGA I/O cell design. (6)

13. (a) (i) Derive Elmore's delay for a RC circuit.

(ii) Discuss the routing resources of ACT1 logic family.

Or

(b) (i) List the important steps and files created in the design of halfgate ASIC using Xilinx software.

(ii) Compare Actel, Xilinx LCA and Altera MAX architectures.

14. (a) Describe how logic synthesis generates smaller and faster circuits with relevant examples. (16)

Or

(b) (i) Describe the boundary scan test. (8)

(ii) Explain the fault simulation and its type. (8)

15. (a) Explain the various techniques used for global routing between and inside flexible blocks. (16)

Or

(b) (i) List the importance of testing. What do you mean by fault modeling? (8)

(ii) Define Built In Self Test. Explain the concept of BIST with example. (8)