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Question Paper Code : 95292

5 Year M.Sc. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Second Semester

Information Technology

EIT 021/ESE 012/ECT 011 — DIGITAL PRINCIPLES

(Common to M.Sc. Computer Technology, M.Sc. Software Engineering and
M.Sc. Software Systems)

(Regulations 2010)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(7575)_8$ to decimal number.
2. Simplify the Boolean function to a minimum member of literals. $XX + XY'$.
3. Implement the function $F = AB + CD + E$ using NAND gates.
4. Sketch a 2-bit binary adder using gates.
5. Differentiate latches and flip-flops.
6. Construct the Excitation table for the T flip flop and RS flip-flop.
7. What are the different types of shift type?
8. What is meant by synchronous counter?
9. Write the methods for designing the control logic.
10. How can the race be avoided?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Express the following function in sum of minterms and products of maxterms. $F(A, B, C, D) = B'D + A'D + ED$. (8)
- (ii) Draw the logic diagram using only two input NOR gates to implement the following expression $Y = (AB + A'B')(CD' + C'D)$. (8)

Or

- (b) Discuss the basic theorems and properties of Boolean Algebra. (16)
12. (a) Using K-map, simplify the Boolean expression given by the function $F(A, B, C, D) = \Sigma(0, 4, 10, 11, 14, 15)$.

Implement the simplified expression using logic gates.

Or

- (b) (i) Design a 4-to-1 multiplexer using logic gates. (8)
- (ii) Implement the function $F(A, B, C) = \Sigma m(0, 3, 5)$ using an 8:1 multiplexer. (8)
13. (a) Describe the operation of magnitude comparator.

Or

- (b) Explain the analysis of clocked sequential circuit with an example.
14. (a) Explain the function of a 4 bit synchronous counter.

Or

- (b) Design a sequence generator to generate the sequence 1011110.
15. (a) (i) Describe the different methods of state assignment.
- (ii) Explain the races with examples.

Or

- (b) Discuss the different hazards and the ways to eliminate them with a neat diagram.