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Question Paper Code : 21686

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Fourth Semester

Instrumentation and Control Engineering

IC 2251/IC 43/EC 1263 A/080260004/10133 IC 403 — DIGITAL PRINCIPLES AND DESIGN

(Regulations 2008/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Implement the following Boolean expression using logic gates.

   (a) $(A + \overline{BC} + AB)$

   (b) $(A' + B).C$

2. State any two differences between encoder and decoder.

3. Show how a JK flip-flop can be operated as a T flip-flop? Apply a 10 KHz square wave as input and determine the output frequency.

4. What is meant by a shift register? List any two types.

5. Design a Half adder using a Multiplexer.

6. What is meant by CPLD?

7. Why is the switching speed of a CMOS greater than NMOS?

8. Specify the power supply grounding considerations for digital ICs.

9. List any two fundamental considerations for design of logic circuit using CMOS.

10. What is Moore's law?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Using the *Quine-McCluskey* method, obtain a simplified sum-of-products expression for the following Boolean function: (10)

$f(a, b, c, d) = \Sigma(0,5,7,8,9,10,11,14,15)$.

(ii) Simplify the following Boolean expression using four-variable K-map:

$F = x'z + w(x'y + xy') + w'xy'$. (6)

Or

(b) (i) Design a Full adder circuit and explain the functioning of the circuit. What relation does it have with the half adder circuit. (10 + 2)

(ii) Realize a EXOR gate using NAND gates only. (4)

12. (a) Design a synchronous decade counter. Draw the logic diagram for a 4 bit Johnson's counter. Sketch the timing diagram and write the sequence in tabular form. (16)

Or

(b) (i) Draw the logic diagram of a JK Flip-flop and explain with its truth table. (12)

(ii) State the difference between a ripple and synchronous counter. (4)

13. (a) (i) An 8 to 1 MUX has inputs AB and C connected to the selection inputs S_2, S_1, S_0 respectively. The data inputs D_0 through D_7 are as follows: $D_1 = D_2 = D_7 = 0$; $D_3 = D_5 = 1$; $D_0 = D_4 = D$, $D_6 = D'$. Determine the Boolean expression that the MUX implements. (10)

(ii) Compare PLA and PAL. (6)

Or

(b) (i) What are the steps used for implementing combinational circuit using PLA? (10)

(ii) Explain FPGA with architecture. (6)

14. (a) Draw and explain the interface of the following:

(i) TTL driving CMOS load. (8)

(ii) CMOS driving TTL load. (8)

Or

(b) (i) List and explain the characteristics of MOS logic families. (8)

(ii) Mention the advantages of ECL over other IC technologies. (8)

15. (a) Design the expression $E = AB' + A'B$ in CMOS. (16)

Or

(b) Design the expression C = (A + B) + AB in CMOS. (16)