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Question Paper Code : 21529

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Fourth Semester

Electronics and Instrumentation Engineering

EI 2253/EI 43/080300014/10133 EE 406 — DIGITAL LOGIC CIRCUITS

(Regulations 2008/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert decimal 65,225 to its hexadecimal and binary equivalents.

2. Simplify the given expression $Y = (A+B)(A+C')(B'+C')$.

3. Draw the logic diagram of a serial adder.

4. Implement $Y = AB + C'D'$ with NAND gates.

5. How could you change an edge-triggered RS flip-flop into an edge-triggered JK flip-flop?

6. What is a ring counter?

7. What is an asynchronous sequential circuit?

8. Give the significance of state assignment.

9. Define the terms: Fan in, Fan out.

10. What is refreshing? How it is done?

PART B — (5 × 16 = 80 marks)

11. (a) Simplify the given Boolean function using K-Map.

(i) $F(A,B,C,D)=\sum m\ (1, 2, 3, 5, 7, 9, 10, 11, 13, 15)$. (8)

(ii) $F(W,X,Y,Z)=WX'Y+WZ+XZ'+YZ'+WY'+WX'$. (8)

Or

(b) Using Quine McCluskey method, simplify the given function.

$F(A,B,C,D)=\sum m\ (2, 3, 7, 9,11, 13) + \sum d(1, 10, 15)$. (16)

12. (a) (i) Design a four bit BCD to excess - 3 code converter and draw the logic diagram. (8)

(ii) Realize $F(a, b, c, d) = \sum (1, 4, 6,7, 8, 9, 10, 11,15)$ using 4- to-1 MUX. (8)

Or

(b) (i) What is a priority encoder? Design a 4-bit priority encoder. (8)

(ii) Design a four hit parallel adder and draw the logic diagram. (8)

13. (a) Design a sequential circuit with four JK Flip-flops ABCD. The next states of B, C, D are equal to the present states of A, B, C. The next state of A is equal to the X-OR of the present states of C and D. (16)

Or

(b) (i) Design a 4-bit bidirectional shift register. (8)

(ii) Design a synchronous counter using JK FF to count the following sequence 7,4, 3,1, 5, 0, 7..... (8)

14. (a) Design an asynchronous sequential circuit that has two inputs X_1, X_2 and one output Z. When $X_1 = 0$, the output Z is 0. The first change in X_2 occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0. (16)

Or

(b) An asynchronous sequential circuit has two internal states and one output. The excitation and output function describing the circuit are as follows.

$Y_1=x_1x_2+x_1y_2+x_2y_1$

$Y_2=x_2+x_1y_1y_2+x_1y_1$

$Z=x_2+y_1$

Draw the logic diagram of the circuit. Obtain the state table, transition table and output map. (16)

15. (a) (i) Explain the operation of two input TTL NAND gate with Totem-pole output. (10)

(ii) Compare PROM, EPROM and EEPROM. (6)

Or

(b) (i) Explain the architecture of FPGA. (8)

(ii) Describe the characteristics of CMOS family. (8)