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Question Paper Code : 21374

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Seventh Semester

Electrical and Electronics Engineering

CS 2071/CS 608/10133 EEE 24 — COMPUTER ARCHITECTURE

(Common to Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)

(Regulations 2008/2010)

(Common to PTCS 2071 — Computer Architecture for B.E. (Part–Time) Sixth Semester — EEE — Regulations 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is Instruction set architecture?
2. What is the function of MAR and MDR?
3. Draw the logic diagram of Half adder.
4. What are the phases of an instruction cycle?
5. State the function of control unit.
6. What is a hazard? What are its types?
7. What is cache memory?
8. List the various memory mapping techniques.
9. What is an interrupt?
10. What is multithreading?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain in detail the various components of computer system with neat diagram. (8)

(ii) Explain in detail the various Data transfer Instructions. (8)

Or

(b) What is an addressing mode? Explain the various addressing modes with suitable examples. (16)

12. (a) Explain floating point adder unit and explain the process addition with a flow chart. (16)

Or

(b) Design a 4 bit Carry look ahead adder and explain its operation with an example. (16)

13. (a) Draw schematic diagram of micro programmed control unit and explain its functioning and compare it with hardwired control unit. (16)

Or

(b) Explain how the instruction pipeline works. What are the various situations where an instruction pipeline can stall? (16)

14. (a) What is address mapping? Explain various mechanisms of mapping main memory address into cache memory addresses. (16)

Or

(b) Discuss in detail about various page replacement policies in virtual memory system. (16)

15. (a) Draw the typical block diagram of a DMA controller and explain how it is used for direct data transfer between memory and peripherals. (16)

Or

(b) What is mean by bus arbitration? Describe bus arbitration daisy chaining and polling schemes for bus arbitration in detail. (16)
