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Question Paper Code : 21505

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Fourth Semester

Electrical and Electronics Engineering

EE 2255/EE 46/EC 1261 A/080280029/10133 EE 406 A — DIGITAL LOGIC CIRCUITS

(Regulations 2008/2010)

(Common to PTEE 2255/10133 EE 406 – Digital Logic Circuits for B.E. (Part-Time) Third Semester – EEE – Regulations 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Give two examples for weighted codes.

2. Define duality principle.

3. What is the drawback in RS flipflop?

4. Write the excitation table for D flipflop.

5. What is state assignment?

6. Give any two applications for asynchronous sequential circuits.

7. What is Fan in and Fan out? Give Fan in, Fan out characteristics of CMOS.

8. What ROM size is needed to implement a binary multiplier that multiplies two 4-bit numbers?

9. Name any two hardware languages.

10. List the features of RTL.

PART B — (5 × 16 = 80 marks)

11. (a) Simplify using Quine McCluskey method

$F(A, B, C, D, E, F) = \Sigma(6, 9, 13, 18, 19, 25, 27, 29, 41, 45, 57, 61)$. (16)

Or

(b) (i) Design a 3-bit magnitude comparator. (8)

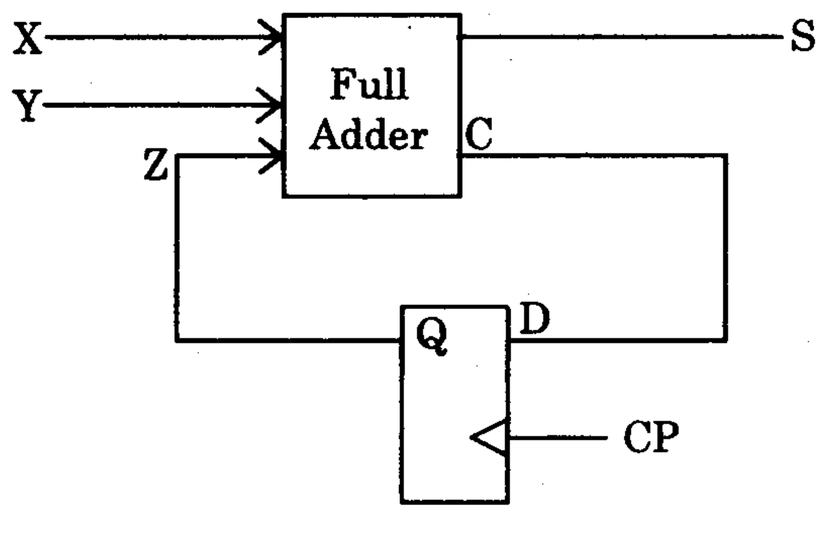
(ii) Design 8421 to excess-3 code converter. (8)

12. (a) (i) Design master-slave flipflop using RS flipflop. (12)

(ii) Draw the logic diagram of clocked D flipflop with AND and NOR gates. (4)

Or

(b) Obtain the state table and state diagram of the sequential circuit. (16)



13. (a) Design mod 5 asynchronous counter. (16)

Or

(b) Design a binary UP-DOWN ripple counter. (16)

14. (a) Design a PLA control circuit for binary multiplier. (16).

Or

(b) Design a circuit that accepts a 3-bit number and generates its square in binary using ROM. (16)

15. (a) Write the VHDL code for Full adder and Full subtractor. Use the Full adder code to implement Binary Parallel Adder (BPA). (16)

Or

(b) Design a VHDL program for mod 12 counter. (16)

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