

LIB
12/1/16 FN

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Question Paper Code : 21376

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Third Semester

Computer Science and Engineering

CS 2202/CS 34/EC 1206 A/080230012/10144 CS 303 – DIGITAL PRINCIPLES AND
SYSTEM DESIGN

(Common to Information Technology)

(Regulations 2008/2010)

(Common to PTCS 2202 – Digital Principles and System Design for B.E. (Part-Time)
Second Semester – CSE – Regulations 2009)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert the gray code (11011) to binary code.
2. Simplify the following expression with Boolean laws.
 $Y = ABC + AB'C + ABC'$
3. What is the drawback of serial adder? For which applications are they preferred?
4. Distinguish between half adder and full adder.
5. Why a multiplexer is called a data selector?
6. How many address bits are needed to operate a $2k \times 8$ bit ROM frequency?
7. Distinguish between synchronous sequential circuits and asynchronous sequential circuits.
8. How many logic devices are required for a MOD-64 parallel counter?
9. State One Hot State Assignment.
10. Compare the ASM chart with a conventional flow chart.

PART B — (5 × 16 = 80 marks)

11. (a) (i) List the ASCII code for the 10 decimal digits with an odd parity in the leftmost position. (6)
- (ii) Simplify the three variable logic expression. (6)
- $$Y = \pi M (1,3,5)$$
- (iii) Implement $Y = (A'B + AB')(C + D')$ using NOR gates. (4)

Or

- (b) Simplify the following Boolean function by using tabulation method. (16)
- $$F(A,B,C,D) = \Sigma(1,4,6,7,8,9,10,11,15)$$
12. (a) (i) With the neat diagram, discuss the working principle of carry look-ahead adder. (11)
- (ii) Design a 4-bit adder using three full adders and one half adder. (5)

Or

- (b) (i) Write the VHDL code for BCD-to-7 segment code convertors, using a selected signal assignment. (12)
- (ii) Write test bench for half adder circuit. (4)
13. (a) (i) Draw the PLA circuit to implement the functions (10)
- $$F_1 = A'B + AC' + A'BC'$$
- $$F_2 = (AC + AB + BC)'$$
- (ii) With the neat sketch, explain the working of RAM cell. (6)

Or

- (b) (i) Write a VHDL code for 2-to-1 multiplexer using if-then-else statement. (10)
- (ii) Derive the circuit for an 8-to-3 priority encoder. (6)
14. (a) A clocked sequential circuit is provided with a single input x and a single output z. Whenever the input produces a string of pulses 111 or 000 and at the end of the sequence it produces an output z = 1 and overlapping is not allowed. (16)
- (i) Obtain the state diagram
- (ii) Obtain the state table
- (iii) Design the sequence detector.

Or

- (b) Using D flip-flops, design a synchronous counter, to count the following repeated binary sequence 0,1,2,4,6. Write the VHDL code for the same. (16)

15. (a) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change for any change in X. Use SR latch for implementation of the circuit. (16)

Or

- (b) (i) With an example explain dynamic and essential hazards. (8)
- (ii) Give the hazard-free realization for the following Boolean functions. (8)
- $f(A,B,C,D) = \Sigma m(1,3,6,7,13,15)$.
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