Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 71540

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2015.

Seventh/Eighth Semester

Electrical and Electronics Engineering

EI 2403/EI 73/10144 EC 605 — VLSI DESIGN

(Common to Instrumentation and Control Engineering/Electronics and Instrumentation Engineering)

(Regulation 2008/2010)

(Common to 10144 EC 605 – VLSI Design for B.E. (Part-Time) Seventh Semester EEE – Regulation 2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is BiCMOS Technology?

2. Compare NMOS and CMOS technology.

3. State lambda based rules for transistor.

4. What are super buffers?

5. Name any one fast adder and fast multiplier.

6. Implement Y = (A + B) (C + D) using NOR-NOR logic.

7. Write the broad classification of PLDs.

8. What do you mean by antifuse technology?

9. Name the data types supported by VHDL.

10. Write the VHDL code for 4 by 1 Multiplexer.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the enhancement and depletion mode of operation of NMOS with their characteristic curves. (10)

(ii) Sketch a typical equivalent circuit model for a MOS transistor. (6)

Or

(b) (i) Obtain the governing equations for NMOS transistor in the linear and saturation regions. (8)

(ii) Write the fabrication steps involved in the CMOS fabrication and how does it differ from BJT fabrication. (8)

12. (a) (i) Explain the voltage transfer characteristics of CMOS inverter. (8)

(ii) Sketch the stick diagram and layout for three input NAND gate. (8)

Or

(b) (i) State the lambda based design rules for wires, transistors and metal contacts. (10)

(ii) Explain and compare CMOS and BiCMOS inverters. (6)

13. (a) (i) Discuss the issues involved in the design of Dynamic CMOS logic. (8)

(ii) Design a tally circuit for three inputs using pass transistor technology. (8)

Or

(b) (i) Implement Y = ABC + DEF using NAND-NAND and AOI logics. (8)

(ii) Explain the functioning of 4 × 4 bit barrel shifter with sketch. (8)

14. (a) (i) Compare PLA and PAL devices. (6)

(ii) Discuss the finite state machine implementation of BCD to Excess 3 code converter in PLA. (10)

Or

(b) Describe the architecture of FPGA with Configurable Logic Block and Programmable interconnect technology.

15. (a) (i) Write the format of PROCESS statement in VHDL. (6)

(ii) Write the VHDL code for 4 bit adder calling full adder as component. (10)

Or

(b) (i) Write short notes on need for Test benches. (6)

(ii) Write the VHDL code for 8 bit counter. (10)