Reg. No. : | | | | | | | | | | |

Question Paper Code: 31056

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2015.

Third Semester

Electronics and Instrumentation Engineering

01UEI306 - DIGITAL ELECTRONICS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. What are the different classifications of binary codes?
2. Reduce A'B'C' + A'BC' + A'BC
3. What is priority encoder?
4. What do you mean by comparator?
5. Define sequential circuit.
6. Define skew and clock skew.
7. What are the various steps to be followed for the design of asynchronous sequential circuit?
8. What is race around condition?
9. Define address and word.
10. Why the input variables to a PAL are buffered?

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Reduce the following function using K-map technique. $f(A,B,C,D) = \prod M(0,2,3,8,9,12,13,15)$ (8)

(ii) Reduce the function to its minimum sum of products form: $Y = \overline{A}\overline{B}\overline{C}D + \overline{A}B\overline{C}D + \overline{A}BCD + \overline{A}BC\overline{D} + AB\overline{C}\overline{D} + AB\overline{C}D + ABCD + A\overline{B}CD$ (8)

Or

(b) Find the minimal sum of product for the Boolean expression, $f = \sum(1,2,3,7,8,9,10,11,14,15)$, using the Quine-McCluskey method. (16)

12. (a) (i) Realise (8)

(a) $Y = A + BC\overline{D}$ Using NAND gate.

(b) $Y = (A+C)(A+\overline{D})(A+B+\overline{C})$ Using NOR gates.

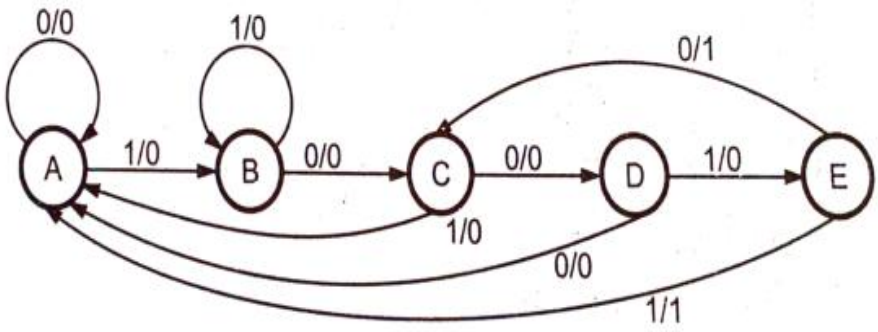
(ii) Implement the Boolean function using 8:1 MUX. $F(P,Q,R,S) = \sum m(0,1,3,4,8,9,15)$ (8)

Or

(b) Design a combinational logic circuit to convert the Gray code into Binary code. (16)

13. (a) (i) Explain how a J-K flip-flop can be converted into a D flip-flop. (8)

(ii) Design a sequential circuit using D flip-flop for the given state diagram. (8)



Or

(b) Design a synchronous BCD counter with J-K Flip-flop. (16)

14. (a) Design an asynchronous sequential circuit with two inputs x_1 and x_2 and one output Z. The output Z=1 if x_1 changes from 0 to 1 , Z=0 if x_2 changes from 0 to 1, and Z=0 otherwise. Realize the circuit using JK flip-flop. (16)

Or

(b) Design a asynchronous circuits that will produce output only the first pulse received and ignore if any other pulses. (16)

15. (a) Explain in detail about the architecture of PLA with a specific example. (16)

Or

(b) Explain the architecture of a RAM with necessary diagrams. (16)

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